When setting up an Asynchronous Transmission, follow these steps:

1. Initialize the SPBRG register for the appropriate baud rate. If a high speed baud rate is desired, set bit BRGH (Section 10.1).
2. Enable the asynchronous serial port by clearing bit SYNC and setting bit SPEN.
3. If interrupts are desired, then set enable bit TXIE.
4. If 9-bit transmission is desired, then set transmit bit TX9.
5. Enable the transmission by setting bit TXEN, which will also set bit TXIF.
6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
7. Load data to the TXREG register (starts transmission).
8. If using interrupts, ensure that GIE and PEIE (bits 7 and 6) of the INTCON register are set.

FIGURE 10-2: ASYNCHRONOUS MASTER TRANSMISSION

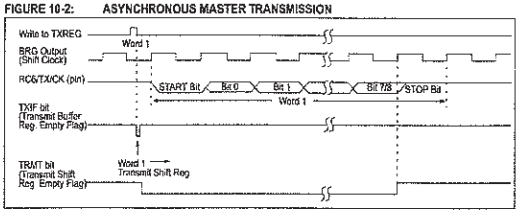
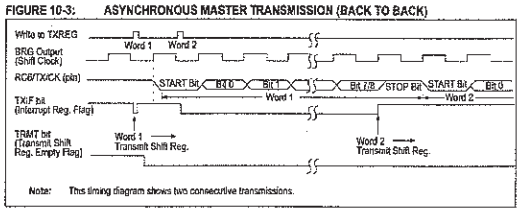


FIGURE 10-3: ASYNCHRONOUS MASTER TRANSMISSION (BACK TO BACK)



Note: This timing diagram shows two consecutive transmissions.

TABLE 10-5: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
0Bh, 8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TOIE	INTE	RBIE	TOIF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF(1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN		FERR	OERR	RX9D	0000 -00x	0000 -00x
19h	TXREG	USART Transmit Register								0000 0000	0000 0000
8Ch	PIE1	PSPIE(1)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC		BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for asynchronous transmission.
Note 1: Bits PSPIE and PSPIF are reserved on the PIC16F873/876; always maintain these bits clear.

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0 0 1 0 0 0 0 0

Right Speed?

12.2 Oscillator Configurations

12.2.1 OSCILLATOR TYPES

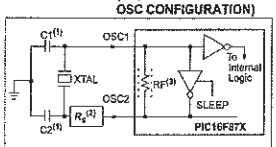
The PIC16F87X can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes:

- LP Low Power Crystal
- XT Crystal/Resonator
- HS High Speed Crystal/Resonator
- RC Resistor/Capacitor

12.2.2 CRYSTAL OSCILLATOR/CERAMIC RESONATORS

In XT, LP or HS modes, a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 12-1). The PIC16F87X oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source to drive the OSC1/CLKIN pin (Figure 12-2).

FIGURE 12-1: CRYSTAL/CERAMIC RESONATOR OPERATION (HS, XT OR LP OSC CONFIGURATION)



Note 1: See Table 12-1 and Table 12-2 for recommended values of C1 and C2.
2: A series resistor (R_S) may be required for AT strip cut crystals.
3: RF varies with the crystal chosen.

FIGURE 12-2: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)

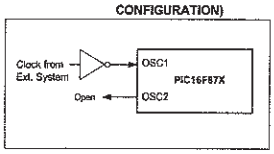


TABLE 12-1: CERAMIC RESONATORS

Ranges Tested:			
Mode	Freq.	OSC1	OSC2
XT	455 kHz	68 - 100 pF	68 - 100 pF
	2.0 MHz	15 - 68 pF	15 - 68 pF
	4.0 MHz	15 - 68 pF	15 - 68 pF
HS	8.0 MHz	10 - 68 pF	10 - 68 pF
	16.0 MHz	10 - 22 pF	10 - 22 pF

These values are for design guidance only. See notes following Table 12-2.

Resonators Used:		
455 kHz	Panasonic EFO-A455K04B	± 0.3%
2.0 MHz	Murata Erie CSA2.00MG	± 0.5%
4.0 MHz	Murata Erie CSA4.00MG	± 0.5%
8.0 MHz	Murata Erie CSA8.00MT	± 0.5%
16.0 MHz	Murata Erie CSA16.00MX	± 0.5%

All resonators used did not have built-in capacitors.

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Tournez la page S.V.P.

TABLE 12-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Osc Type	Crystal Freq.	Cap. Range C1	Cap. Range C2
LP	32 kHz	33 pF	33 pF
	200 kHz	15 pF	15 pF
XT	200 kHz	47-68 pF	47-68 pF
	1 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	8 MHz	15-33 pF	15-33 pF
	20 MHz	15-33 pF	15-33 pF

These values are for design guidance only. See notes following this table.

Crystals Used		
32 kHz	Epson C-001R32.768K-A	± 20 PPM
200 kHz	STD XTL 200.000KHz	± 20 PPM
1 MHz	ECS ECS-10-13-1	± 50 PPM
4 MHz	ECS ECS-40-20-1	± 50 PPM
8 MHz	EPSON CA-301 8.000M-C	± 30 PPM
20 MHz	EPSON CA-301 20.000M-C	± 30 PPM

Note 1: Higher capacitance increases the stability of oscillator, but also increases the start-up time.

2: Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.

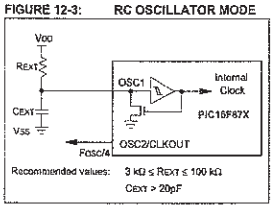
3: R_S may be required in HS mode, as well as XT mode, to avoid overdriving crystals with low drive level specification.

4: When migrating from other PICmicro devices, oscillator performance should be verified.

12.2.3 RC OSCILLATOR

For timing insensitive applications, the "RC" device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low CEXT values. The user also needs to take into account variation due to tolerance of external R and C components used. Figure 12-3 shows how the R/C combination is connected to the PIC16F87X.

FIGURE 12-3: RC OSCILLATOR MODE



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15.2 DC Characteristics: PIC16F873/874/876/877-04 (Commercial, Industrial) PIC16F873/874/876/877-20 (Commercial, Industrial) PIC16LF873/874/876/877-04 (Commercial, Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature −40°C ≤ TA ≤ +85°C for industrial 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD range as described in DC specification (Section 15.1)				
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	VIL	**Input Low Voltage**					
		I/O ports					
D030		with TTL buffer	VSS	—	0.15VDD	V	For entire VDD range
D030A			VSS	—	0.8V	V	4.5V ≤ VDD ≤ 5.5V
D031		with Schmitt Trigger buffer	VSS	—	0.2VDD	V	
D032		MCLR, OSC1 (in RC mode)	VSS	—	0.2VDD	V	
D033		OSC1 (in XT, HS and LP)	VSS	—	0.3VDD	V	(Note 1)
		Ports RC3 and RC4		—			
D034		with Schmitt Trigger buffer	VSS	—	0.3VDD	V	For entire VDD range
D034A		with SMBus	-0.5	—	0.6	V	for VDD = 4.5 to 5.5V
	VIH	**Input High Voltage**					
		I/O ports		—			
D040		with TTL buffer	2.0	—	VDD	V	4.5V ≤ VDD ≤ 5.5V
D040A			0.25VDD + 0.8V	—	VDD	V	For entire VDD range
D041		with Schmitt Trigger buffer	0.8VDD	—	VDD	V	For entire VDD range
D042		MCLR	0.8VDD	—	VDD	V	
D042A		OSC1 (XT, HS and LP)	0.7VDD	—	VDD	V	(Note 1)
D043		OSC1 (in RC mode)	0.9VDD	—	VDD	V	
		Ports RC3 and RC4					
D044		with Schmitt Trigger buffer	0.7VDD	—	VDD	V	For entire VDD range
D044A		with SMBus	1.4	—	5.5	V	for VDD = 4.5 to 5.5V
D070	IPURB	**PORTB Weak Pull-up Current**	50	250	400	µA	VDD = 5V, VPIN = VSS, -40°C TO +85°C
	IIL	**Input Leakage Current**(2, 3)					
D060		I/O ports	—	—	±1	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
D061		MCLR, RA4/T0CKI	—	—	±5	µA	VSS ≤ VPIN ≤ VDD
D063		OSC1	—	—	±5	µA	VSS ≤ VPIN ≤ VDD, XT, HS and LP osc configuration

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16F87X be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

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15.2 DC Characteristics: PIC16F873/874/876/877-04 (Commercial, Industrial) PIC16F873/874/876/877-20 (Commercial, Industrial) PIC16LF873/874/876/877-04 (Commercial, Industrial) (Continued)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD range as described in DC specification (Section 15.1)				
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	VOL	**Output Low Voltage**					
D080		I/O ports	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C
D083		OSC2/CLKOUT (RC osc config)	—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C
	VOH	**Output High Voltage**					
D090		I/O ports(3)	VDD - 0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C
D092		OSC2/CLKOUT (RC osc config)	VDD - 0.7	—	—	V	IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C
D150*	VOD	**Open-Drain High Voltage**	—	—	8.5	V	RA4 pin
		Capacitive Loading Specs on Output Pins					
D100	COSC2	OSC2 pin	—	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1
D101	CIO	All I/O pins and OSC2 (RC mode)	—	—	50	pF	
D102	CB	SCL, SDA (I^2C mode)	—	—	400	pF	
		Data EEPROM Memory					
D120	ED	Endurance	100K	—	—	E/W	25°C at 5V
D121	VDRW	VDD for read/write	VMIN	—	5.5	V	Using EECON to read/write VMIN = min. operating voltage
D122	TDEW	Erase/write cycle time	—	4	8	ms	
		Program FLASH Memory					
D130	EP	Endurance	1000	—	—	E/W	25°C at 5V
D131	VPR	VDD for read	VMIN	—	5.5	V	VMIN = min operating voltage
D132A		VDD for erase/write	VMIN	—	5.5	V	Using EECON to read/write, VMIN = min. operating voltage
D133	TPEW	Erase/Write cycle time	—	4	8	ms	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16F87X be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

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6. Documentation XBEE

1. XBee®/XBee-PRO® RF Modules

The XBee and XBee-PRO RF Modules were engineered to meet IEEE 802.15.4 standards and support the unique needs of low-cost, low-power wireless sensor networks. The modules require minimal power and provide reliable delivery of data between devices.

The modules operate within the ISM 2.4 GHz frequency band and are pin-for-pin compatible with each other.

Key Features

Long Range Data Integrity

XBee

- Indoor/Urban: up to 100' (30 m)
- Outdoor line-of-sight: up to 300' (90 m)
- Transmit Power: 1 mW (0 dBm)
- Receiver Sensitivity: -92 dBm

XBee-PRO

- Indoor/Urban: up to 300' (90 m), 200' (60 m) for International variant
- Outdoor line-of-sight: up to 1 mile (1600 m), 2500' (750 m) for International variant
- Transmit Power: 63mW (18dBm), 10mW (10dBm) for International variant
- Receiver Sensitivity: -100 dBm

RF Data Rate: 250,000 bps

Advanced Networking & Security

Retries and Acknowledgements

DSSS (Direct Sequence Spread Spectrum)

Each direct sequence channels has over 65,000 unique network addresses available

Source/Destination Addressing

Unicast & Broadcast Communications

Point-to-point, point-to-multipoint and peer-to-peer topologies supported

Low Power

XBee

- TX Peak Current: 45 mA (@3.3 V)
- RX Current: 50 mA (@3.3 V)
- Power-down Current: < 10 µA

XBee-PRO

- TX Peak Current: 250mA (150mA for international variant)
- TX Peak Current (RPSMA module only): 340mA (180mA for international variant)
- RX Current: 55 mA (@3.3 V)
- Power-down Current: < 10 µA

ADC and I/O line support

Analog-to-digital conversion, Digital I/O

I/O Line Passing

Easy-to-Use

No configuration necessary for out-of box RF communications

Free X-CTU Software (Testing and configuration software)

AT and API Command Modes for configuring module parameters

Extensive command set

Small form factor

Worldwide Acceptance

FCC Approval (USA) Refer to Appendix A [p64] for FCC Requirements. Systems that contain XBee®/XBee-PRO® RF Modules inherit Digi Certifications.

ISM (Industrial, Scientific & Medical) **2.4 GHz frequency band**

Manufactured under **ISO 9001:2000** registered standards

XBee®/XBee-PRO® RF Modules are optimized for use in the United States, Canada, Australia, Japan, and Europe. Contact Digi for complete list of government agency approvals.

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Specifications

Table 1-01. Specifications of the XBee®/XBee-PRO® RF Modules

Performance		
Indoor/Urban Range	Up to 100 ft (30 m)	Up to 300 ft (90 m), up to 200 ft (60 m) International variant
Outdoor RF line-of-sight Range	Up to 300 ft (90 m)	Up to 1 mile (1600 m), up to 2500 ft (750 m) International variant
Transmit Power Output (software selectable)	1mW (0 dBm)	63mW (18dBm)* 10mW (10 dBm) for International variant
RF Data Rate	250,000 bps	250,000 bps
Serial Interface Data Rate (software selectable)	1200 bps - 250 kbps (non-standard baud rates also supported)	1200 bps - 250 kbps (non-standard baud rates also supported)
Receiver Sensitivity	-92 dBm (1% packet error rate)	-100 dBm (1% packet error rate)
Power Requirements		
Supply Voltage	2.8 – 3.4 V	2.8 – 3.4 V
Transmit Current (typical)	45mA (@ 3.3 V)	250mA (@3.3 V) (150mA for International variant) RPSMA module only: 340mA (@3.3 V) (180mA for international variant)
Idle / Receive Current (typical)	50mA (@ 3.3 V)	55mA (@ 3.3 V)
Power-down Current	< 10 µA	< 10 µA
General		
Operating Frequency	ISM 2.4 GHz	ISM 2.4 GHz
Dimensions	0.960" x 1.087" (2.438cm x 2.761cm)	0.960" x 1.227" (2.438cm x 3.294cm)
Operating Temperature	-40 to 85° C (industrial)	-40 to 85° C (industrial)
Antenna Options	Integrated Whip, Chip or U.FL Connector, RPSMA Connector	Integrated Whip, Chip or U.FL Connector, RPSMA Connector
Networking & Security		
Supported Network Topologies	Point-to-point, Point-to-multipoint & Peer-to-peer	
Number of Channels (software selectable)	16 Direct Sequence Channels	12 Direct Sequence Channels
Addressing Options	PAN ID, Channel and Addresses	PAN ID, Channel and Addresses
Agency Approvals		
United States (FCC Part 15.247)	OUR-XBEE	OUR-XBEEPRO
Industry Canada (IC)	4214A-XBEE	4214A-XBEEPRO
Europe (CE)	ETSI	ETSI (Max. 10 dBm transmit power output)*
Japan	R201WW07215214	R201WW08215111 (Max. 10 dBm transmit power output)*
Australia	C-Tick	C-Tick

* See Appendix A for region-specific certification requirements.

Antenna Options: The ranges specified are typical when using the integrated Whip (1.5 dBi) and Dipole (2.1 dBi) antennas. The Chip antenna option provides advantages in its form factor; however, it typically yields shorter range than the Whip and Dipole antenna options when transmitting outdoors. For more information, refer to the "XBee Antennas" Knowledgebase Article located on Digi's Support Web site

Mechanical Drawings

Figure 1-01. Mechanical drawings of the XBee®/XBee-PRO® RF Modules (antenna options not shown)

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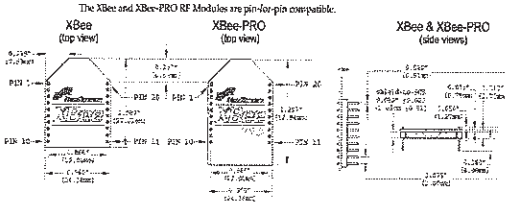
The XBee and XBee-PRO RF Modules are pin-for-pin compatible.



Pin Signals

Figure 1-01. XBee®/XBee-PRO® RF Module Pin Numbers
(top side shown - shields on bottom)

Table 1-02. Pin Assignments for the XBee and XBee-PRO Modules
(Low-asserted signals are distinguished with a horizontal line above signal name.)

Pin #	Name	Direction	Description
1	VCC	-	Power Supply
2	DOUT	Output	UART Data Out
3	DIN / CONFIG	Input	UART Data In
4	DIO12	Output	Digital Output 0
5	RESET	Input	Module Reset (reset pulse must be at least 200 ns)
6	PWM0 / RSSI	Output	PWM Output 0 / RX Signal Strength Indicator
7	PWM1	Output	PWM Output 1
8	Reserved	-	Do not connect
9	DTR / SLEEP_RQ / DI8	Input	Pin Sleep Control Line or Digital Input 8
10	GND	-	Ground
11	AD4 / DIO4	Either	Analog Input 4 or Digital I/O 4
12	CTS / DIO7	Either	Clear-to-Send Flow Control or Digital I/O 7
13	ON / SLEEP	Output	Module Status Indicator
14	VREF	Input	Voltage Reference for A/D Inputs
15	Associate / AD5 / DIO5	Either	Associated Indicator, Analog Input 5 or Digital I/O 5
16	RTS / AD6 / DIO6	Either	Request-to-Send Flow Control, Analog Input 6 or Digital I/O 6
17	AD3 / DIO3	Either	Analog Input 3 or Digital I/O 3
18	AD2 / DIO2	Either	Analog Input 2 or Digital I/O 2
19	AD1 / DIO1	Either	Analog Input 1 or Digital I/O 1
20	AD0 / DIO0	Either	Analog Input 0 or Digital I/O 0

* Function is not supported at the time of this release

Design Notes:

- Minimum connections: VCC, GND, DOUT & DIN
- Minimum connections for updating firmware: VCC, GND, DIN, DOUT, RTS & DTR
- Signal Direction is specified with respect to the module
- Module includes a 50k Ω pull-up resistor attached to RESET
- Several of the input pull-ups can be configured using the PR command
- Unused pins should be left disconnected

Electrical Characteristics

Table 1-03. DC Characteristics (VCC = 2.8 - 3.4 VDC)

V_{IL}	Input Low Voltage	All Digital Inputs	-	-	0.35 * VCC	V
V_{IH}	Input High Voltage	All Digital Inputs	0.7 * VCC	-	-	V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA, VCC >= 2.7 V	-	-	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -2 mA, VCC >= 2.7 V	VCC - 0.5	-	-	V
I_{IR}	Input Leakage Current	V_{IN} = VCC or GND, all inputs, per pin	-	0.025	1	µA
I_{OZ}	High Impedance Leakage Current	V_{IN} = VCC or GND, all I/O High-Z, per pin	-	0.025	1	µA
TX	Transmit Current	VCC = 3.3 V	-	45 (XBee)	215, 149 (PRO, Int)	mA
RX	Receive Current	VCC = 3.3 V	-	50 (XBee)	55 (PRO)	mA
PWR-DWN	Power-down Current	SM parameter = 1	-	< 10	-	µA

Table 1-04. ADC Characteristics (Operating)

V_{REFH}	VREF - Analog-to-Digital converter reference range		2.08	-	V_{DDAD}*	V
I_{REF}	VREF - Reference Supply Current	Enabled	-	200	-	µA
		Disabled or Sleep Mode	-	< 0.01	0.02	µA
V_{AIDC}	Analog Input Voltage[1]		V_{SSAD} - 0.3	-	V_{DDAD} + 0.3	V

1. Maximum electrical operating range, not valid conversion range.
* V_{DDAD} is connected to VCC.

Table 1-05. ADC Timing/Performance Characteristics[1]

R_{AS}	Source Impedance at Input[2]		-	-	10	kΩ
V_{AIN}	Analog Input Voltage[3]		V_{REFL}		V_{REFH}	V
RES	Ideal Resolution (1 LSB)[4]	$2.09V \leq V_{DDAD} \leq 3.6V$	2.031	-	3.516	mV
DNL	Differential Non-linearity[5]		-	±0.5	±1.0	LSB
E_{IL}	Integral Non-linearity[6]		-	±0.5	±1.0	LSB
E_{ZS}	Zero-scale Error[7]		-	±0.4	±1.0	LSB
E_{FS}	Full-scale Error[8]		-	±0.4	±1.0	LSB
E_{IL}	Input Leakage Error[9]		-	±0.05	±5.0	LSB
E_{TU}	Total Unadjusted Error[10]		-	±1.1	±2.5	LSB

1. All ACCURACY numbers are based on processor and system being in WAIT state (very little activity and no IO switching) and that adequate low-pass filtering is present on analog input pins (filter with 0.01 µF to 0.1 µF capacitor between analog input and VREFL). Failure to observe these guidelines may result in system or microcontroller noise causing accuracy errors which will vary based on board layout and the type and magnitude of the activity.
Data transmission and reception during data conversion may cause some degradation of these specifications, depending on the number and timing of packets. It is advisable to test the ADCs in your installation if best accuracy is required.
2. R_{AS} is the real portion of the impedance of the network driving the analog input pin. Values greater than this amount may not fully charge the input circuitry of the ATD resulting in accuracy error.
3. Analog input must be between V_{REFL} and V_{REFH} for valid conversion. Values greater than V_{REFH} will convert to 3FF.
4. The resolution is the ideal step size or 1LSB = (V_{REFH}-V_{REFL})/1024
5. Differential non-linearity is the difference between the current code width and the ideal code width (1LSB). The current code width is the difference in the transition voltages to and from the current code.
6. Integral non-linearity is the difference between the transition voltage to the current code and the adjusted ideal transition voltage for the current code. The adjusted ideal transition voltage is (Current Code−1/2)*(1/(((V_{REFH}+E_{FS})−(V_{REFL}+E_{ZS})))).
7. Zero-scale error is the difference between the transition to the first valid code and the ideal transition to that code. The ideal transition voltage to a given code is (Code−1/2)*(1/(V_{REFH}−V_{REFL})).
8. Full-scale error is the difference between the transition to the last valid code and the ideal transition to that code. The ideal transition voltage to a given code is (Code−1/2)*(1/(V_{REFH}−V_{REFL})).
9. Input leakage error is error due to input leakage across the real portion of the impedance of the network driving the analog pin. Reducing the impedance of the network reduces this error.

Tournez la page S.V.P.

2. RF Module Operation

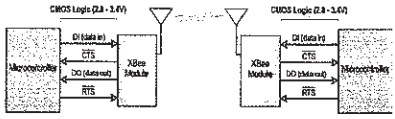
Serial Communications

The XBee®/XBee-PRO® RF Modules interface to a host device through a logic-level asynchronou serial port. Through its serial port, the module can communicate with any logic and voltage com patible UART; or through a level translator to any serial device (For example: Through a Digi pro prietary RS-232 or USB interface board).

UART Data Flow

Devices that have a UART interface can connect directly to the pins of the RF module as shown i the figure below.

Figure 2-01. System Data Flow Diagram in a UART-interfaced environment
(Low-asserted signals distinguished with horizontal line over signal name.)

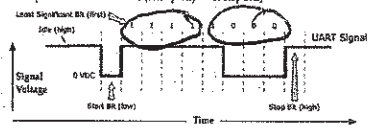


Serial Data

Data enters the module UART through the DI pin (pin 3) as an asynchronous serial signal. The sig nal should idle high when no data is being transmitted.

Each data byte consists of a start bit (low), 8 data bits (least significant bit first) and a stop bit (high). The following figure illustrates the serial bit pattern of data passing through the module.

Figure 2-02. UART data packet 0x1F (decimal number "31") as transmitted through the RF module
Example Data Format is 8-N-1 (bits - parity - # of stop bits)

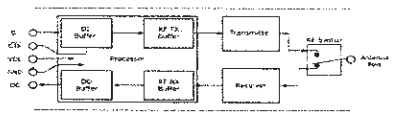


Serial communications depend on the two UARTs (the microcontroller's and the RF module's) to b configured with compatible settings (baud rate, parity, start bits, stop bits, data bits).

The UART baud rate and parity settings on the XBee module can be configured with the BD and SI commands, respectively. See the command table in Chapter 3 for details.

Flow Control

Figure 2-03. Internal Data Flow Diagram



DI (Data In) Buffer

When serial data enters the RF module through the DI pin (pin 3), the data is stored in the DI Buf fer until it can be processed.

Hardware Flow Control ($\overline{CTS}$). When the DI buffer is 17 bytes away from being full; by default, the module de-asserts $\overline{CTS}$ (high) to signal to the host device to stop sending data [refer to D7 (DIO7 Configuration) parameter]. $\overline{CTS}$ is re-asserted after the DI Buffer has 34 bytes of memory available.

How to eliminate the need for flow control:

1. Send messages that are smaller than the DI buffer size (202 bytes).
2. Interface at a lower baud rate [BD (Interface Data Rate) parameter] than the throughput data rate.

Case in which the DI Buffer may become full and possibly overflow:

If the module is receiving a continuous stream of RF data, any serial data that arrives on the DI pin is placed in the DI Buffer. The data in the DI buffer will be transmitted over-the-air when the module is no longer receiving RF data in the network.

Refer to the RO (Packetization Timeout), BD (Interface Data Rate) and D7 (DIO7 Configuration) com mand descriptions for more information.

DO (Data Out) Buffer

When RF data is received, the data enters the DO buffer and is sent out the serial port to a hos device. Once the DO Buffer reaches capacity, any additional incoming RF data is lost.

Hardware Flow Control ($\overline{RTS}$). If $\overline{RTS}$ is enabled for flow control (D6 (DIO6 Configuration) Parameter = 1), data will not be sent out the DO Buffer as long as $\overline{RTS}$ (pin 16) is de-asserted.

Two cases in which the DO Buffer may become full and possibly overflow:

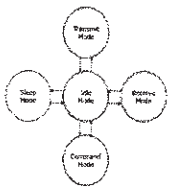
1. If the RF data rate is set higher than the interface data rate of the module, the module w receive data from the transmitting module faster than it can send the data to the host.
2. If the host does not allow the module to transmit data out from the DO buffer because i being held off by hardware or software flow control.

Refer to the D6 (DIO6 Configuration) command description for more information.

Modes of Operation

XBee®/XBee-PRO® RF Modules operate in five modes.

Figure 2-07. Modes of Operation



Idle Mode

When not receiving or transmitting data, the RF module is in Idle Mode. The module shifts into the other modes of operation under the following conditions:

- Transmit Mode (Serial data is received in the DI Buffer)
- Receive Mode (Valid RF data is received through the antenna)
- Sleep Mode (Sleep Mode condition is met)
- Command Mode (Command Mode Sequence is issued)

Transmit/Receive Modes

RF Data Packets

Each transmitted data packet contains a Source Address and Destination Address field. The Source Address matches the address of the transmitting module as specified by the MY (Source Address) parameter (if MY >= 0xFFFE), the SH (Serial Number High) parameter or the SL (Serial Number Low) parameter. The <Destination Address> field is created from the DH (Destination Address High) and DL (Destination Address Low) parameter values. The Source Address and/or Destination Address fields will either contain a 16-bit short or long 64-bit long address.

The RF data packet structure follows the 802.15.4 specification.

[Refer to the XBee/XBee-PRO Addressing section for more information]

Direct and Indirect Transmission

There are two methods to transmit data:

- Direct Transmission - data is transmitted immediately to the Destination Address
- Indirect Transmission - A packet is retained for a period of time and is only transmitted after the destination module (Source Address = Destination Address) requests the data.

Indirect Transmissions can only occur on a Coordinator. Thus, if all nodes in a network are End Devices, only Direct Transmissions will occur. Indirect Transmissions are useful to ensure packet delivery to a sleeping node. The Coordinator currently is able to retain up to 2 indirect messages.

Sleep Mode

Sleep Modes enable the RF module to enter states of low-power consumption when not in use. In order to enter Sleep Mode, one of the following conditions must be met (in addition to the module having a non-zero SM parameter value):

- Sleep_RQ (pin 9) is asserted and the module is in a pin sleep mode (SM = 1, 2, or 5)
- The module is idle (no data transmission or reception) for the amount of time defined by the ST (Time before Sleep) parameter. [NOTE: ST is only active when SM = 4-5.]

Table 2-04. Sleep Mode Configurations

Pin Hibernate (SM = 1)	Asserd (high) Sleep_RQ (pin 9)	De-assert (low) Sleep_RQ	Pin/Host-controlled / Non-Beacon systems only / Lowest Power	(SM)	< 10 µA (@3.0 VCC)
Pin Doze (SM = 2)	Asserd (high) Sleep_RQ (pin 9)	De-assert (low) Sleep_RQ	Pin/Host-controlled / Non-Beacon systems only / Fastest wake-up	(SM)	< 50 µA
Cyclic Sleep (SM = 4)	Automatic transition to Sleep Mode as defined by the SM (Sleep Mode) and ST (Time before Sleep) parameters	Transition occurs after the cyclic sleep time interval elapses. The time interval is defined by the SP (Cyclic Sleep Period) parameter.	RF module wakes in pre-determined time intervals to detect if RF data is present / When SM = 6	(SM), SP, ST	< 50 µA when sleeping
Cyclic Sleep (SM = 5)	Automatic transition to Sleep Mode as defined by the SM (Sleep Mode) and ST (Time before Sleep) parameters or or on a falling edge transition of the SLEEP_RQ pin.	Transition occurs after the cyclic sleep time interval elapses. The time interval is defined by the SP (Cyclic Sleep Period) parameter.	RF module wakes in pre-determined time intervals to detect if RF data is present. Module also wakes on a falling edge of SLEEP_RQ	(SM), SP, ST	< 50 µA when sleeping

The SM command is central to setting Sleep Mode configurations. By default, Sleep Modes are disabled (SM = 0) and the module remains in Idle/Receive Mode. When in this state, the module is constantly ready to respond to serial or RF activity.

Pin/Host-controlled Sleep Modes

The transient current when waking from pin sleep (SM = 1 or 2) does not exceed the idle current of the module. The current ramps up exponentially to its idle current.

Pin Hibernate (SM = 1)

- Pin/Host-controlled
- Typical power-down current: < 10 µA (@3.0 VCC)
- Wake-up time: 13.2 msec

Pin Hibernate Mode minimizes quiescent power (power consumed when in a state of rest or inactivity). This mode is voltage level-activated; when Sleep_RQ (pin 9) is asserted, the module will finish any transmit, receive or association activities, enter Idle Mode, and then enter a state of sleep. The module will not respond to either serial or RF activity while in pin sleep.

To wake a sleeping module operating in Pin Hibernate Mode, de-assert Sleep_RQ (pin 9). The module will wake when Sleep_RQ is de-asserted and is ready to transmit or receive when the CTS line is low. When waking the module, the pin must be de-asserted at least two 'byte times' after CTS goes low. This assures that there is time for the data to enter the DI buffer.

Pin Doze (SM = 2)

- Pin/Host-controlled
- Typical power-down current: < 50 µA
- Wake-up time: 2 msec

Pin Doze Mode functions as does Pin Hibernate Mode; however, Pin Doze features faster wake-up time and higher power consumption.

To wake a sleeping module operating in Pin Doze Mode, de-assert Sleep_RQ (pin 9). The module will wake when Sleep_RQ is de-asserted and is ready to transmit or receive when the CTS line is

Command Mode

To modify or read RF Module parameters, the module must first enter into Command Mode – a state in which incoming characters are interpreted as commands. Two Command Mode options are supported: AT Command Mode [refer to section below] and API Command Mode [p57].

AT Command Mode

To Enter AT Command Mode:

Send the 3-character command sequence "+++" and observe guard times before and after the command characters. [Refer to the "Default AT Command Mode Sequence" below.]

Default AT Command Mode Sequence (for transition to Command Mode):

- No characters sent for one second [GT (Guard Times) parameter = 0x3E8]
- Input three plus characters ("+++") within one second [CC (Command Sequence Character) parameter = 0x2B.]
- No characters sent for one second [GT (Guard Times) parameter = 0x3E8]

All of the parameter values in the sequence can be modified to reflect user preferences.

NOTE: Failure to enter AT Command Mode is most commonly due to baud rate mismatch. Ensure the 'Baud' setting on the "PC Settings" tab matches the interface data rate of the RF module. By default, the BD parameter = 3 (9600 bps).

To Send AT Commands:

Send AT commands and parameters using the syntax shown below.

Figure 2-08. Syntax for sending AT Commands

Example: ATDL 1F<CR>

To read a parameter value stored in the RF module's register, omit the parameter field.

The preceding example would change the RF module Destination Address (Low) to "0x1F". To store the new value to non-volatile (long term) memory, subsequently send the WR (Write) command.

For modified parameter values to persist in the module's registry after a reset, changes must be saved to non-volatile memory using the WR (Write) Command. Otherwise, parameters are restored to previously saved values after the module is reset.

System Response. When a command is sent to the module, the module will parse and execute the command. Upon successful execution of a command, the module returns an "OK" message. If execution of a command results in an error, the module returns an "ERROR" message.

To Exit AT Command Mode:

1. Send the ATCN (Exit Command Mode) command (followed by a carriage return).
   [OR]
2. If no valid AT Commands are received within the time specified by CT (Command Mode Timeout) Command, the RF module automatically returns to Idle Mode.

For an example of programming the RF module using AT Commands and descriptions of each configurable parameter, refer to the RF Module Configuration chapter [p26].

* Firmware version in which the command was first introduced (firmware versions are numbered in hexadecimal notation.)

Serial Interfacing

Table 3-05. XBee-PRO Commands - Serial Interfacing

BD	Serial Interfacing	Interface Data Rate. Set/Read the serial interface data rate for communications between the RF module serial port and host. Request non-standard baud rates with values above 0x80 using a terminal window. Read the BD register to find actual baud rate achieved.	0 - 7 (standard baud rates) 0 = 1200 bps 1 = 2400 2 = 4800 3 = 9600 4 = 19200 5 = 38400 6 = 57600 7 = 115200 0x80 - 0x2DC6C0 (non-standard baud rates up to 250 Kbps)	3
RO	Serial Interfacing	Packetization Timeout. Set/Read number of character times of inter-character delay required before transmission. Set to zero to transmit characters as they arrive instead of buffering them into one RF packet.	0 - 0xFF [x character times]	3
AP (v1.x80*)	Serial Interfacing	API Enable. Disable/Enable API Mode.	0 - 2 0 =Disabled 1 = API enabled 2 = API enabled (escaped control characters)	0
NB	Serial Interfacing	Parity. Set/Read parity settings.	0 - 4 0 = 8-bit no parity 1 = 8-bit even 2 = 8-bit odd 3 = 8-bit mark 4 = 8-bit space	0
PR (v1.x80*)	Serial Interfacing	Pull-up Resistor Enable. Set/Read bitfield to configure internal pull-up resistor status for I/O lines Bitfield Map. bit 0 - AD4/DIO4 (pin11) bit 1 - AD3 / DIO3 (pin17) bit 2 - AD2/DIO2 (pin18) bit 3 - AD1/DIO1 (pin19) bit 4 - AD0 / DIO0 (pin20) bit 5 - RTS / AD6 / DIO6 (pin16) bit 6 - DTR / SLEEP_RQ / DI8 (pin9) bit 7 - DIN/CONFIG (pin3) Bit set to "1" specifies pull-up enabled; "0" specifies no pull-up	0 - 0xFF	0xFF

* Firmware version in which the command was first introduced (firmware versions are numbered in hexadecimal notation.)

I/O Settings

Table 3-06. XBee-PRO Commands - I/O Settings (sub-category designated within [brackets])

D8	I/O Settings	DI8 Configuration. Select/Read options for the DI8 line (pin 9) of the RF module.	0 - 1 0 = Disabled 3 = DI (1,2,4 & 5 n/a)	0
D7 (v1.x80*)	I/O Settings	DIO7 Configuration. Select/Read settings for the DIO7 line (pin 12) of the RF module. Options include CTS flow control and I/O line settings.	0 - 1 0 = Disabled 1 = CTS Flow Control 2 = (n/a) 3 = DI 4 = DO low 5 = DO high 6 = RS485 Tx Enable Low 7 = RS485 Tx Enable High	1
D6 (v1.x80*)	I/O Settings	DIO6 Configuration. Select/Read settings for the DIO6 line (pin 16) of the RF module. Options include RTS flow control and I/O line settings.	0 - 1 0 = Disabled 1 = RTS flow control 2 = (n/a) 3 = DI 4 = DO low 5 = DO high	0

Command Descriptions

Command descriptions in this section are listed alphabetically. Command categories are designated within "< >" symbols that follow each command title. XBee®/XBee-PRO® RF Modules expect parameter values in hexadecimal (designated by the "0x" prefix).

All modules operating within the same network should contain the same firmware version.

A1 (End Device Association) Command

<Networking {Association}> The A1 command is used to set and read association options for an End Device.

Use the table below to determine End Device behavior in relation to the A1 parameter.

AT Command: ATA1

Parameter Range: 0 - 0x0F [bitfield]

Default Parameter Value: 0

Related Commands: ID (PAN ID), NI (Node Identifier), CH (Channel), CE (Coordinator Enable), A2 (Coordinator Association)

Minimum Firmware Version Required: v1.x80

0 - ReassignPanID	0 - Will only associate with Coordinator operating on PAN ID that matches Node Identifier
	1 - May associate with Coordinator operating on any PAN ID
1 - ReassignChannel	0 - Will only associate with Coordinator operating on Channel that matches CH setting
	1 - May associate with Coordinator operating on any Channel
2 - AutoAssociate	0 - Device will not attempt Association
	1 - Device attempts Association until success Note: This bit is used only for Non-Beacon systems. End Devices in a Beaconing system must always associate to a Coordinator
3 - PollCoordOnPinWake	0 - Pin Wake will not poll the Coordinator for pending (indirect) Data
	1 - Pin Wake will send Poll Request to Coordinator to extract any pending data
4 - 7	[reserved]

A2 (Coordinator Association) Command

<Networking {Association}> The A2 command is used to set and read association options of the Coordinator.

Use the table below to determine Coordinator behavior in relation to the A2 parameter.

AT Command: ATA2

Parameter Range: 0 - 7 [bitfield]

Default Parameter Value: 0

Related Commands: ID (PAN ID), NI (Node Identifier), CH (Channel), CE (Coordinator Enable), A1 (End Device Association), AS Active Scan), ED (Energy Scan)

Minimum Firmware Version Required: v1.x80

0 - ReassignPanID	0 - Coordinator will not perform Active Scan to locate available PAN ID. It will operate on ID (PAN ID).
	1 - Coordinator will perform Active Scan to determine an available ID (PAN ID). If a PAN ID conflict is found, the ID parameter will change.
1 - ReassignChannel	0 - Coordinator will not perform Energy Scan to determine free channel. It will operate on the channel determined by the CH parameter.
	1 - Coordinator will perform Energy Scan to find a free channel, then operate on that channel.
2 - AllowAssociate	0 - Coordinator will not allow any devices to associate to it.
	1 - Coordinator will allow devices to associate to it.
3 - 7	[reserved]

The binary equivalent of the default value (0x06) is 00000110. 'Bit 0' is the last digit of the sequence.

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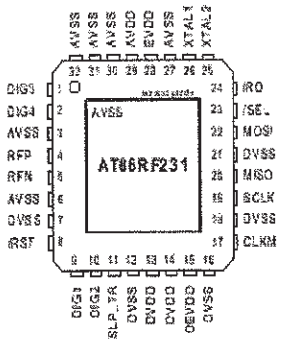
7. Documentation AT86RF231

Features

- High Performance RF-CMOS 2.4 GHz Radio Transceiver Targeted for IEEE 802.15 ZigBee®, 6LoWPAN, RF4CE, SP100, WirelessHART™ and ISM Applications
- Industry Leading Link Budget (104 dB)
  - Receiver Sensitivity -101 dBm
  - Programmable Output Power from -17 dBm up to +3 dBm
- Ultra-Low Current Consumption:
  - SLEEP = 0.02 µA
  - TRX_OFF = 0.4 mA
  - RX_ON = 12.3 mA
  - BUSY_TX = 14 mA (at max. Transmit Power of +3 dBm)
- Ultra-Low Supply Voltage (1.8V to 3.6V) with Internal Regulator
- Optimized for Low BoM Cost and Ease of Production:
  - Few External Components Necessary (Crystal, Capacitors and Antenna)
  - Excellent ESD Robustness
- Easy to Use Interface:
  - Registers, Frame Buffer and AES Accessible through Fast SPI
  - Only Two Microcontroller GPIO Lines Necessary
  - One Interrupt Pin from Radio Transceiver
  - Clock Output with Prescaler from Radio Transceiver
- Radio Transceiver Features:
  - 128-byte FIFO (SRAM) for Data Buffering
  - Programmable Clock Output, to Clock the Host Microcontroller or as Timer Reference
  - Integrated RX/TX Switch
  - Fully Integrated, Fast Settling PLL to support Frequency Hopping
  - Battery Monitor
  - Fast Wake-Up Time < 0.4 msec
- Special IEEE 802.15.4-2006 Hardware Support:
  - FCS Computation and Clear Channel Assessment
  - RSSI Measurement, Energy Detection and Link Quality Indication
- MAC Hardware Accelerator:
  - Automated Acknowledgement, CSMA-CA and Retransmission
  - Automatic Address Filtering
  - Automated FCS Check
- Extended Feature Set Hardware Support:
  - AES 128-bit Hardware Accelerator
  - RX/TX Indication (external RF Front-End Control)
  - RX Antenna Diversity
  - Supported PSDU data rates: 250 kb/s, 500 kb/s, 1 Mb/s and 2 Mb/s
  - True Random Number Generation for Security Application
- Industrial and Extended Temperature Range:
  - -40°C to +85°C and -40°C to +125°C
- I/O and Packages:
  - 32-pin Low-Profile QFN Package 5 x 5 x 0.9 mm³
  - RoHS/Fully Green
- Compliant to IEEE 802.15.4-2006 and IEEE 802.15.4-2003
- Compliant to EN 300 328/440, FCC-CFR-47 Part 15, ARIB STD-T66, RSS-210

1. Pin-out Diagram

Figure 1-1. AT86RF231 Pin-out Diagram



Note: The exposed paddle is electrically connected to the die inside the package. It shall be soldered to the board to ensure electrical and thermal contact and good mechanical stability.

1.1 Pin Descriptions

Table 1-1. Pin Description AT86RF231

Pins	Name	Type	Description
1	DIG3	Digital output (Ground)	1. RX/TX indicator, see Section 11.5 2. If disabled, pull-down enabled (AVSS)
2	DIG4	Digital output (Ground)	1. RX/TX indicator (DIG3 inverted), see Section 11.5 2. If disabled, pull-down enabled (AVSS)
3	AVSS	Ground	Ground for RF signals
4	RFP	RF I/O	Differential RF signal
5	RFN	RF I/O	Differential RF signal
6	AVSS	Ground	Ground for RF signals
7	DVSS	Ground	Digital ground
8	/RST	Digital input	Chip reset; active low
9	DIG1	Digital output (Ground)	1. Antenna Diversity RF switch control, see Section 11.4 2. If disabled, pull-down enabled (DVSS)
10	DIG2	Digital output (Ground)	1. Antenna Diversity RF switch control (DIG1 inverted), see Section 11.4 2. Signal IRQ_2 (RX_START) for RX Frame Time Stamping, see Section 11.6 3. If functions disabled, pull-down enabled (DVSS)
11	SLP_TR	Digital input	Controls sleep, transmit start, receive states; active high, see Section 6.5
12	DVSS	Ground	Digital ground
13	DVDD	Supply	Regulated 1.8V voltage regulator; digital domain, see Section 9.4
14	DVDD	Supply	Regulated 1.8V voltage regulator; digital domain, see Section 9.4
15	DEVDD	Supply	External supply voltage; digital domain
16	DVSS	Ground	Digital ground
17	CLKM	Digital output	Master clock signal output; low if disabled, see Section 9.6
18	DVSS	Ground	Digital ground
19	SCLK	Digital input	SPI clock
20	MISO	Digital output	SPI data output (Master Input Slave Output)
21	DVSS	Ground	Digital ground
22	MOSI	Digital input	SPI data input (Master Output Slave Input)
23	/SEL	Digital input	SPI select, active low
24	IRQ	Digital output	1. Interrupt request signal: active high or active low; configurable 2. Frame Buffer Empty Indicator; active High, see Section 11.7
25	XTAL2	Analog input	Crystal pin, see Section 9.5
26	XTAL1	Analog input	Crystal pin or external clock supply, see Section 9.5
27	AVSS	Ground	Analog ground
28	EVDD	Supply	External supply voltage, analog domain

Table 1-1. Pin Description AT86RF231 (Continued)

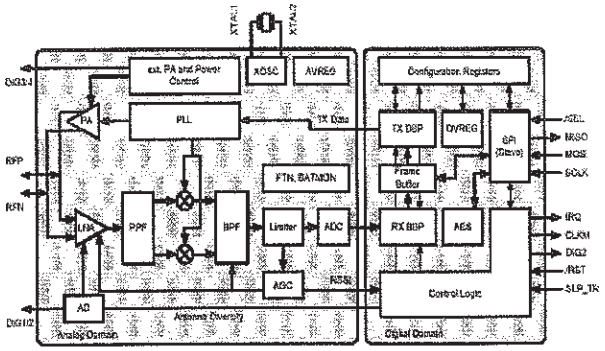
Pins	Name	Type	Description
29	AVDD	Supply	Regulated 1.8V voltage regulator; analog domain, see Section 9.4
30	AVSS	Ground	Analog ground
31	AVSS	Ground	Analog ground
32	AVSS	Ground	Analog ground
Paddle	AVSS	Ground	Analog ground; Exposed paddle of QFN package

4. General Circuit Description

This single-chip radio transceiver provides a complete radio transceiver interface between an antenna and a microcontroller. It comprises the analog radio, digital modulation and demodulation including time and frequency synchronization and data buffering. The number of external components is minimized such that only the antenna, the crystal and decoupling capacitors are required. The bidirectional differential antenna pins (RFP, RFN) are used for transmission and reception, thus no external antenna switch is needed.

The AT86RF231 block diagram is shown in Figure 4-1 on page 10.

Figure 4-1. AT86RF231 Block Diagram



The received RF signal at pins RFN and RFP is differentially fed through the low-noise amplifier (LNA) to the RF filter (PPF) to generate a complex signal, driving the integrated channel filter (BPF). The limiting amplifier provides sufficient gain to drive the succeeding analog-to-digital converter (ADC) and generates a digital RSSI signal. The ADC output signal is sampled by the digital base band receiver (RX BBP).

The transmit modulation scheme is offset-QPSK (O-QPSK) with half-sine pulse shaping and 32-length block coding (spreading) according to [1] and [2]. The modulation signal is generated in the digital transmitter (TX BBP) and applied to the fractional-N frequency synthesis (PLL), to ensure the coherent phase modulation required for demodulation of O-QPSK signals. The frequency-modulated signal is fed to the power amplifier (PA).

A differential pin pair DIG3/DIG4 can be enabled to control an external RF front-end.

Two on-chip low-dropout voltage regulators (A|DVREG) provide the analog and digital 1.8V supply.

An internal 128-byte RAM for RX and TX (Frame Buffer) buffers the data to be transmitted or the received data.

The configuration of the AT86RF231, reading and writing of Frame Buffer is controlled by the SPI interface and additional control lines.

The AT86RF231 further contains comprehensive hardware-MAC support (Extended Operating Mode) and a security engine (AES) to improve the overall system power efficiency and timing. The stand-alone 128-bit AES engine can be accessed in parallel to all PHY operational transactions and states using the SPI interface, except during SLEEP state.

For applications not necessarily targeting IEEE 802.15.4 compliant networks, the radio transceiver also supports alternative data rates up to 2 Mb/s.

For long-range applications or to improve the reliability of an RF connection the RF performance can further be improved by using an external RF front-end or Antenna Diversity. Both operation modes are supported by the AT86RF231 with dedicated control pins without the interaction of the microcontroller.

Additional features of the Extended Feature Set, see Section 11. "AT86RF231 Extended Feature Set" on page 128, are provided to simplify the interaction between radio transceiver and microcontroller.

9.6 Crystal Oscillator (XOSC)

The main crystal oscillator features are:

- 16 MHz amplitude controlled crystal oscillator
- 330 µs typical settling time after leaving SLEEP state
- Configurable trimming capacitance array
- Configurable clock output (CLKM)

9.6.1 Overview

The crystal oscillator generates the reference frequency for the AT86RF231. All other internally generated frequencies of the radio transceiver are derived from this unique frequency. Therefore, the overall system performance is mainly determined by the accuracy of crystal reference frequency. The external components of the crystal oscillator should be selected carefully and the related board layout should be done with caution (see Section 5. "Application Circuits" on page 12).

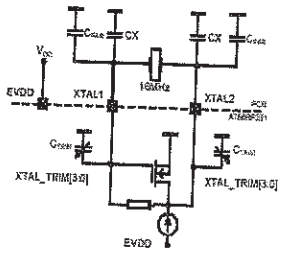
The register 0x12 (XOSC_CTRL) provides access to the control signals of the oscillator. Two operating modes are supported. It is recommended to use the integrated oscillator setup as described in Figure 9-7 on page 116; nevertheless a reference frequency can be fed to the internal circuitry by using an external clock reference as shown in Figure 9-8 on page 117.

9.6.2 Integrated Oscillator Setup

Using the internal oscillator, the oscillation frequency depends on the load capacitance between the crystal pins XTAL1 and XTAL2. The total load capacitance C_L must be equal to the specified load capacitance of the crystal itself. It consists of the external capacitors CX and parasitic capacitances connected to the XTAL nodes.

Figure 9-7 on page 116 shows all parasitic capacitances, such as PCB stray capacitances and the pin input capacitance, summarized to C_{PAR}.

Figure 9-7. Simplified XOSC Schematic with External Components



Additional internal trimming capacitors C_{TRIM} are available. Any value in the range from 0 pF to 4.5 pF with a 0.3 pF resolution is selectable using XTAL_TRIM of register 0x12 (XOSC_CTRL).

To calculate the total load capacitance, the following formula can be used:

$C_L = 0.5 * (CX + C_{TRIM} + C_{PAR})$.

The trimming capacitors provide the possibility of reducing frequency deviations caused by production process variations or by external components tolerances. Note that the oscillation frequency can only be reduced by increasing the trimming capacitance. The frequency deviation caused by one step of C_{TRIM} decreases with increasing crystal load capacitor values.

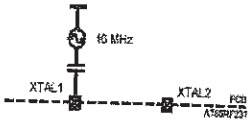
An amplitude control circuit is included to ensure stable operation under different operating conditions and for different crystal types. Enabling the crystal oscillator in P_ON state and after leaving SLEEP state causes a slightly higher current during the amplitude build-up phase to guarantee a short start-up time. At stable operation, the current is reduced to the amount necessary for a robust operation. This also keeps the drive level of the crystal low.

Generally, crystals with a higher load capacitance are less sensitive to parasitic pulling effects caused by external component variations or by variations of board and circuit parasitics. On the other hand, a larger crystal load capacitance results in a longer start-up time and a higher steady state current consumption.

9.6.3 External Reference Frequency Setup

When using an external reference frequency, the signal must be connected to pin 28 (XTAL1) as indicated in Figure 9-8 on page 117 and the register bits XTAL_MODE (register 0x12, XOSC_CTRL) need to be set to the external oscillator mode. The oscillation peak-to-peak amplitude shall be between 100 mV and 500 mV, the optimum range is between 400 mV and 500 mV. Pin 25 (XTAL2) should not be wired.

Figure 9-8. Setup for Using an External Frequency Reference



9.6.4 Master Clock Signal Output (CLKM)

The generated reference clock signal can be fed to a microcontroller using pin 17 (CLKM). The internal 16 MHz raw clock can be divided by an internal prescaler. Thus, clock frequencies of 16 MHz, 8 MHz, 4 MHz, 2 MHz, 1 MHz, 250 kHz, or 62.5 kHz can be supplied by pin CLKM.

The CLKM frequency, update scheme, and pin driver strength is configurable using register 0x03 (TRX_CTRL_0). There are two possibilities how a CLKM frequency change gets effective. If CLKM_SHA_SEL = 0 and/or CLKM_CTRL = 0, changing the register bits CLKM_CTRL immediately affects the CLKM clock rate. Otherwise (CLKM_SHA_SEL = 1 and CLKM_CTRL > 0 before changing the register bits CLKM_CTRL) the new clock rate is supplied when leaving the SLEEP state the next time.

To reduce power consumption and spurious emissions, it is recommended to turn off the CLKM clock when not in use or to reduce its driver strength to a minimum, refer to Section 1.3 "Digital Pins" on page 7.

9.7 Frequency Synthesizer (PLL)

The main PLL features are:

- Generate RX/TX frequencies for all IEEE 802.15.4 - 2.4 GHz channels
- Autonomous calibration loops for stable operation within the operating range
- Two PLL-interrupts for status indication
- Fast PLL settling to support frequency hopping

9.7.1 Overview

The PLL generates the RF frequencies for the AT86RF231. During receive operation the frequency synthesizer works as a local oscillator on the radio transceiver receive frequency, during transmit operation the voltage-controlled oscillator (VCO) is directly modulated to generate the RF transmit signal. The frequency synthesizer is implemented as a fractional-N PLL.

Two calibration loops ensure correct PLL functionality within the specified operating limits.

9.7.2 RF Channel Selection

The PLL is designed to support 16 channels in the 2.4 GHz ISM band with a channel spacing of 5 MHz according to IEEE 802.15.4. The center frequency of these channels is defined as follows:

$F_c = 2405 + 5\ (k - 11)$ in [MHz], for k = 11, 12,..., 26

where k is the channel number.

The channel k is selected by register bits CHANNEL (register 0x08, PHY_CC_CA).

9.7.3 Frequency Agility

When the PLL is enabled during state transition from TRX_OFF to PLL_ON, the settling time is typically t_{PLL} = 110 µs, including settling of the analog voltage regulator (AVREG) and PLL self calibration, refer to Table 7-2 on page 43 and Figure 13-13 on page 169. A lock of the PLL is indicated with an interrupt IRQ_0 (PLL_LOCK).

Switching between 2.4 GHz ISM band channels in PLL_ON or RX_ON states is typically done within $t_{PLL,CH}$ = 11 µs. This makes the radio transceiver highly suitable for frequency hopping applications.

When starting the transmit procedure the PLL frequency is changed to the transmit frequency within a period of t_{PLS} = 16 µs before starting the transmission. After the transmission the PLL settles back to the receive frequency within a period of t_{PLS} = 32 µs. This frequency step does not generate an interrupt IRQ_0 (PLL_LOCK) or IRQ_1 (PLL_UNLOCK) within these periods.

9.7.4 Calibration Loops

Due to variation of temperature, supply voltage and part-to-part variations of the radio transceiver the VCO characteristics may vary.

To ensure a stable operation, two automated control loops are implemented, center frequency (CF) tuning and delay cell (DCU) calibration. Both calibration loops are initiated automatically when the PLL is enabled during state transition from TRX_OFF to PLL_ON state. Additionally, center frequency calibration is initiated when the PLL changes to a different channel center frequency.

If the PLL operates for a long time on the same channel, e.g. more than 5 min, or the operating temperature changes significantly, it is recommended to initiate the calibration loops manually.

Both calibration loops can be initiated manually by setting PLL_CF_START = 1 (register 0x1A, PLL_CF) and register bit PLL_DCU_START = 1 (register 0x1B, PLL_DCU). To start the calibration the device must be in PLL_ON or RX_ON state. The completion of the center frequency tuning is indicated by a PLL_LOCK interrupt.

Both calibration loops may be run simultaneously.

9.7.5 Interrupt Handling

Two different interrupts indicate the PLL status (refer to register 0x0F). IRQ_0 (PLL_LOCK) indicates that the PLL has locked. IRQ_1 (PLL_UNLOCK) interrupt indicates an unexpected unlock condition. A PLL_LOCK interrupt clears any preceding PLL_UNLOCK interrupt automatically and vice versa.

A PLL_LOCK interrupt is supposed to occur in the following situations:

- State change from TRX_OFF to PLL_ON / RX_ON / TX_ARET_ON / RX_AACK_ON
- Channel change in states PLL_ON / RX_ON / TX_ARET_ON / RX_AACK_ON

Any other occurrences of PLL interrupts indicate erroneous behavior and require checking of the actual device status.

The state transition from BUSY_TX to PLL_ON after successful transmission does not generate an IRQ_0 (PLL_LOCK) within the settling period.

9.7.6 Register Description

Register 0x08 (PHY_CC_CCA):

This register sets the IEEE 802.15.4 - 2.4 GHz channel number

Bit	7	6	5	4	3	2	1	0
0x08	CCA REQUEST	CCA MODE		CHANNEL				PHY_CC_CCA
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	1	0	1	1	1	1

- Bit 7 - CCA_REQUEST

Refer to Section 8.5 "Clear Channel Assessment (CCA)" on page 94.

- Bit [6:5] - CCA_MODE

Refer to Section 8.5 "Clear Channel Assessment (CCA)" on page 94.

- Bit [4:0] - CHANNEL

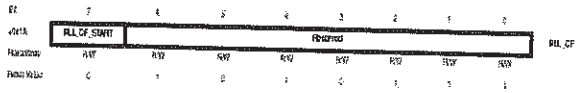
The register bits CHANNEL define the RX/TX channel. The channel assignment is according to IEEE 802.15.4.

Table 9-17. Channel Assignment for IEEE 802.15.4 - 2.4 GHz Band

Register Bit	Value	Channel Number *k*	Center Frequency [MHz]
CHANNEL	0x0B	11	2405
	0x0C	12	2410
	0x0D	13	2415
	0x0E	14	2420
	0x0F	15	2425
	0x10	16	2430
	0x11	17	2435
	0x12	18	2440
	0x13	19	2445
	0x14	20	2450
	0x15	21	2455
	0x16	22	2460
	0x17	23	2465
	0x18	24	2470
	0x19	25	2475
	0x1A	26	2480

Register 0x1A (PLL_CF):

This register controls the operation of the center frequency calibration loop.



- Bit 7 - PLL_CF_START

PLL_CF_START = 1 initiates the center frequency calibration. The calibration cycle has finished after t_{PLL_CF} = 85 µs (typ.). The register bit is cleared immediately after finishing the calibration.

- Bit [6:0] - Reserved

Register 0x1B (PLL_DCU):

This register controls the operation of the delay cell calibration loop.

- Bit 7 - PLL_DCU_START

PLL_DCU_START = 1 initiates the delay cell calibration. The calibration cycle has finished after at most t_{PLL_DCU} = 6 µs, the register bit is set to 0. The register bit is cleared immediately after finishing the calibration.

- Bit [6:0] - Reserved