Control Time Slot 1, Status Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**0**	**0**	**1**	**MLB**	**OLB**	**CLB**	**RSRV**	
Reset (R)	0	0	1	0	0	1	X	X

BIT	NAME	VALUE		FUNCTION
RSRV	Reserved Bits			Must be written as 0.
CLB	Control Latch Bit	1	*R*	Ensures proper transition between control and data mode.
OLB	Output Level Bit	0	*R*	Line full scale outputs are 2.8 Vpp (1Vrms) Headphone full scale output is 4.0 Vpp. Speaker full scale output is 8.0 Vpp.
		1		Line and Headphone full scale outputs are 2.0 Vpp. Speaker full scale output is 4.0 Vpp.
MLB	Microphone Level	0	*R*	20 dB Fixed Gain Enabled Full scale microphone inputs are 0.288 Vpp.
		1		20 dB Fixed Gain Disabled Full scale inputs are 2.88 Vpp.

Control Time Slot 2, Data Format Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**HPF**	**RSRV**	**DFR2**	**DFR1**	**DFR0**	**ST**	**DF1**	**DF0**
Reset (R)	0	X	0	0	0	0	0	1

BIT	NAME	VALUE			FUNCTION		
DF1-0	Data Format Selection	0 0	0		16-bit 2's-complement linear.		
		0 1	1	*R*	8-bit μ–Law.		
		1 0	2		8-bit A-Law.		
		1 1	3		8-bit unsigned linear.		
ST	Stereo Bit	0		*R*	Mono Mode.		
		1			Stereo Mode.		
DFR2-0	Data Conversion Frequency Selection				CLKIN (÷)	XTAL1(kHz) 24.576 MHz	XTAL2 (kHz) 16.9344 MHz
		0 0 0	0	*R*	3072	8	5.5125
		0 0 1	1		1536	16	11.025
		0 1 0	2		896	27.42857	18.9
		0 1 1	3		768	32	22.05
		1 0 0	4		448	NA	37.8
		1 0 1	5		384	NA	44.1
		1 1 0	6		512	48	33.075
		1 1 1	7		2560	9.6	6.615
RSRV	Reserved Bit				Must be written as 0		
HPF	High Pass Filter	0		*R*	Disabled.		
		1			Enabled. A Digital High Pass Filter is used to force the ADC DC offset to zero.		

Control Time Slot 3, Serial Port Control Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**ITS**	**MCK2**	**MCK1**	**MCK0**	**BSEL1**	**BSEL0**	**XCLK**	**XEN**
Reset (R)	0	0	0	0	1	0	0	1

BIT	NAME	VALUE			FUNCTION
XEN	Transmitter Enable	0			Enable the serial data output.
		1		*R*	Disable (high-impedance state) serial data output.
XCLK	Transmit Clock	0		*R*	Receive SCLK and FSYNC from external source SLAVE Mode
		1			Generate SCLK and FSYNC MASTER Mode
BSEL1-0	Select Bit Rate	0 0	0		64 bits per frame.
		0 1	1		128 bits per frame.
		1 0	2	*R*	256 bits per frame.
		1 1	3		Reserved.
MCK2-0	Clock Source Select	0 0 0	0	*R*	SCLK is master clock, 256 bits per frame. BSEL must equal 2, and XCLK must equal 0.
		0 0 1	1		XTAL1, 24.576 MHz, is clock source.
		0 1 0	2		XTAL2, 16.9344 MHz, is clock source.
		0 1 1	3		CLKIN is clock source, and must be 256xFs.
		1 0 0	4		CLKIN is clock source, DFR2-0 select sample frequency.
ITS	Immediate Three-State	0		*R*	SCLK and FSYNC three-state up to 12 clocks after D/C goes low.
		1			SCLK and FSYNC three-state immediately after D/C goes low.

Control Time Slot 4, Test Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**TEST**						**ENL**	**DAD**
Reset (R)	0	0	0	0	0	0	0	0

BIT	NAME	VALUE		FUNCTION
DAD	Loopback Mode	0	*R*	Digital-Digital Loopback.
		1		Digital-Analog-Digital Loopback.
ENL	Enable Loopback Testing	0	*R*	Disable.
		1		Enable.
TEST	Test bits			The TEST bits must be written as zero, otherwise special factory test modes may be invoked.

Control Time Slot 5, Parallel Port Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register	PIO1	PIO0	RSRV					
Reset (R)	1	1	X	X	X	X	X	X

BIT	NAME	VALUE	FUNCTION
RSRV	Reserved Bits		Must be written as 0.
PIO1-0	Parallel I/O Bits	1 1 3 R	See the Parallel Input/Output Section.

Control Time Slot 6, Reserved Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register	RSRV							
Reset (R)	X	X	X	X	X	X	X	X

BIT	NAME	VALUE	FUNCTION
RSRV	Reserved Bits		Must be written as 0.

Control Time Slot 7, Version Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register	RSRV				VER3	VER2	VER1	VER0
Reset (R)	X	X	X	X	0	0	1	0

BIT	NAME	VALUE	FUNCTION
VER3-0	Device Version Number	0 0 0 0 0 0 0 0 1 1 0 0 1 0 2 R	"C". See *Appendix A.* "D". See *Appendix A.* "E". This Data Sheet
RSRV	Reserved Bits		Must be written as 0.

Control Time Slot 8, Reserved Register

	D7	D6	D5	D4	D3	D2	D1	D0
Register	RSRV							
Reset (R)	X	X	X	X	X	X	X	X

BIT	NAME	VALUE	FUNCTION
RSRV	Reserved Bits		Must be written as 0.

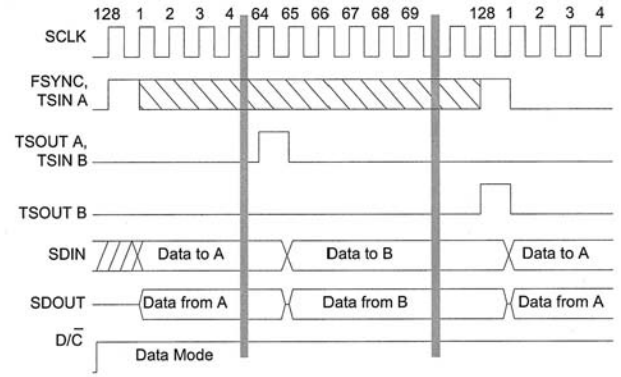

Figure 12. Data Mode Timing for 2 CS4215's

DATA MODE

The data mode is used during conversions to pass digital data between the CS4215 and external devices. The frame sync rate is equal to the value of the conversion frequency set by the DFR2-DFR0 bits of the Data Format register. Each frame has either 64, 128, or 256 bit times depending on the BSEL bits in the Serial Control register. Control of gain, attenuation, input selection and output muting are embedded in the data stream.

Time slot	Description
1	Left Audio MS8 bits
2	Left Audio LS8 bits
3	Right Audio MS8 bits
4	Right Audio LS8 bits
5	Output Setting
6	Output Setting
7	Input Setting
8	Input Setting

Table 2. Data Registers

Data Formats

All time slots contain 8 bits. The MSB of the data is transmitted/received first. The CS4215 data registers have the functions and time slot assignments shown in Table 2. The register address is the time slot number when D/$\overline{C}$ is 1. The SDOUT pin goes into a high-impedance state prior to time slot 1 and after Time Slot 8 (see Figure 12).

The CS4215 supports four audio data formats: 16-bit 2's-complement linear, 8-bit unsigned linear, 8-bit A-Law, and 8-bit μ-Law. Figure 13 illustrates the transfer characteristic for 16-bit and 8-bit linear formats. Note that a digital code

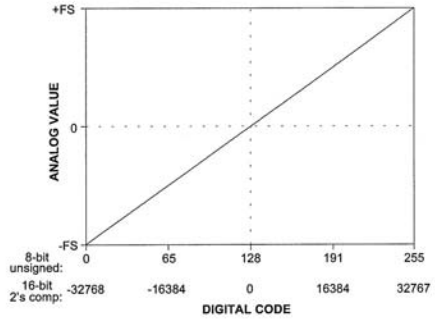

Figure 13. Linear Data Formats

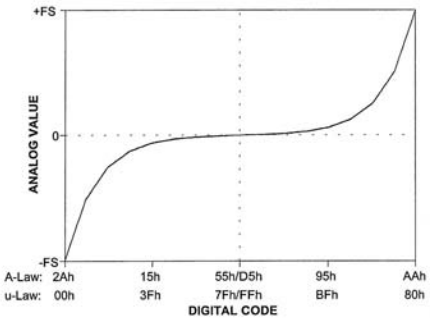

Figure 14. Companded Data Formats

of 128 (80 Hex) is considered analog zero for the 8-bit unsigned format.

A non-linear coding scheme is used for the companded formats as shown in Figure 14. This scheme is compatible with CCITT G.711. Companding uses more precision at lower amplitudes at the expense of less precision at higher amplitudes. μ-Law is equivalent to 13 bits at low signal levels and A-Law is equivalent to 12 bits. This low-level dynamic range is obtained at the expense of large-signal dynamic range which, for both μ-Law and A-Law, is equivalent to 6 bits. The CS4215 internally operates at 16 bits. The companded data is expanded to the upper 13 (12) bits for the DACs and compressed from the upper 13 (12) bits to 8 bits for the ADCs.

Data Time Slot 1&2, Left Channel Audio Data

Time slot 1 and 2 contain audio data for the left channel. In mono modes, only the left channel data is used, however both the right and left output DACs are driven. In 8-bit modes, only time slot 1 is used for the data.

Data Time Slot 3&4, Right Channel Audio Data

Time slot 3 and 4 contains audio data for the right channel. In mono modes, the right ADC outputs zero and the right DAC uses the left digital data. In 8-bit modes, only time slot 3 is used for the data.

Figure 15 summarizes all the time slot bit allocations for the 4 data modes and for control mode.

Reset

$\overline{\text{RESET}}$ going low causes all the internal control registers to be set to the states shown with each register description. $\overline{\text{RESET}}$ must be brought low and high at least once after power up. $\overline{\text{RESET}}$ returning high causes the CS4215 to execute an offset calibration cycle. $\overline{\text{RESET}}$ or D/$\overline{\text{C}}$ returning high should occur at least 50 ms after the power supply has stabilized to allow the voltage reference to settle.

Data Time Slot 5, Output Setting

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**HE**	**LE**	**LO5**	**LO4**	**LO3**	**LO2**	**LO1**	**LO0**
Reset (R)	0	0	1	1	1	1	1	1

BIT	NAME	VALUE		FUNCTION
LO5-0	Left Channel Output Attenuation Setting	1 1 1 1 1 1 63	*R*	1.5dB attenuation steps. LO5 is the MSB. 0 = no attenuation. 111111 = -94.5dB
LE	Line Output Enable	0 1	*R*	Analog line outputs off (muted). Analog line outputs on.
HE	Headphone Output Enable	0 1	*R*	Headphone output off (muted). Headphone output on.

Data Time Slot 6, Output Setting

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**ADI**	**SE**	**RO5**	**RO4**	**RO3**	**RO2**	**RO1**	**RO0**
Reset (R)	1	0	1	1	1	1	1	1

BIT	NAME	VALUE		FUNCTION
RO5-0	Right Channel Output Attenuation Setting	1 1 1 1 1 1 63	*R*	1.5dB attenuation steps. RO5 is the MSB. 0 = no attenuation. 111111 = -94.5dB Not used in mono modes.
SE	Speaker Enable	0 1	*R*	Speaker off (muted). Speaker on.
ADI	A/D Data Invalid	0 1	*R*	A/D data valid. A/D data invalid. Busy in calibration.

Data Time Slot 7, Input Setting

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**PIO1**	**PIO0**	**OVR**	**IS**	**LG3**	**LG2**	**LG1**	**LG0**
Reset (R)	1	1	0	0	0	0	0	0

BIT	NAME	VALUE		FUNCTION
LG3-0	Left Channel Input Gain Setting	0 0 0 0	*R*	1.5dB gain steps. LG3 is the MSB. 0 = no gain, 1111 = 22.5dB gain.
IS	Input Select	0 1	*R*	Line level inputs (LINL, LINR). Microphone level inputs (MINL, MINR).
OVR	Overrange	0	*R*	When read as 1, this bit indicates that an input over-range condition has occurred. The bit remains set until cleared by writing 0 into the register. Writing a 1 enables the overrange detection. The bit will remain 0 until an over-range occurs. Serial port clear has priority over internal settings.
PIO1-0	Parallel I/O	1 1	3 *R*	Parallel input/output bits.

Data Time Slot 8, Input Setting

	D7	D6	D5	D4	D3	D2	D1	D0
Register	**MA3**	**MA2**	**MA1**	**MA0**	**RG3**	**RG2**	**RG1**	**RG0**
Reset (R)	1	1	1	1	0	0	0	0

BIT	NAME	VALUE		FUNCTION
RG3-0	Right Channel Input Gain Setting	0 0 0 0	*R*	1.5dB gain steps. RG3 is the MSB. 0 = no gain, 1111 = 22.5dB gain.
MA3-0	Monitor Path Attenuation	1 1 1 1 15	*R*	6dB attenuation steps. MA3 is the MSB. 0 = no attenuation, 1111 = mute.

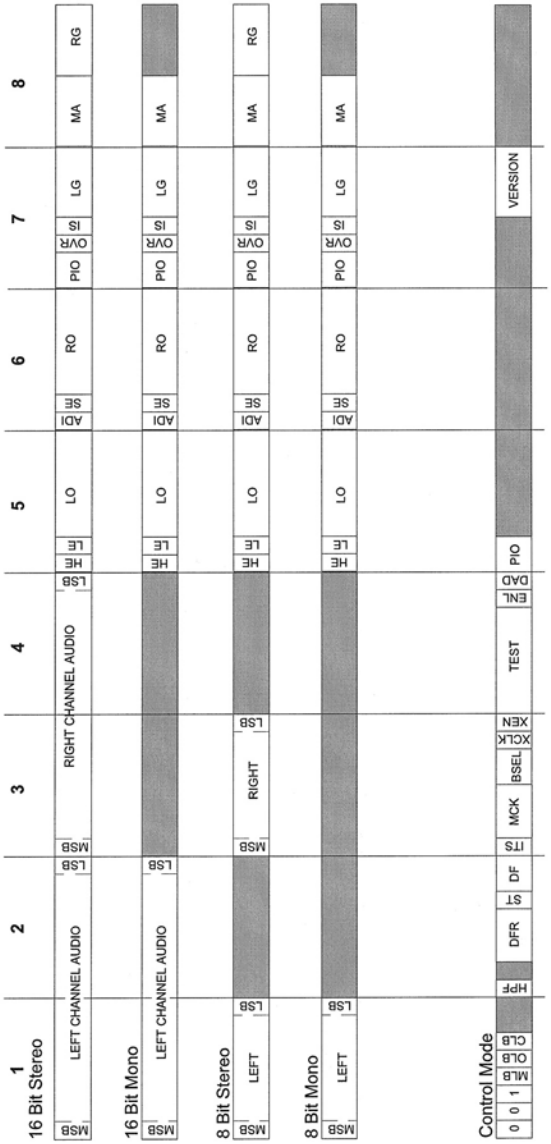

Figure 15. Time Slot/Register Overview

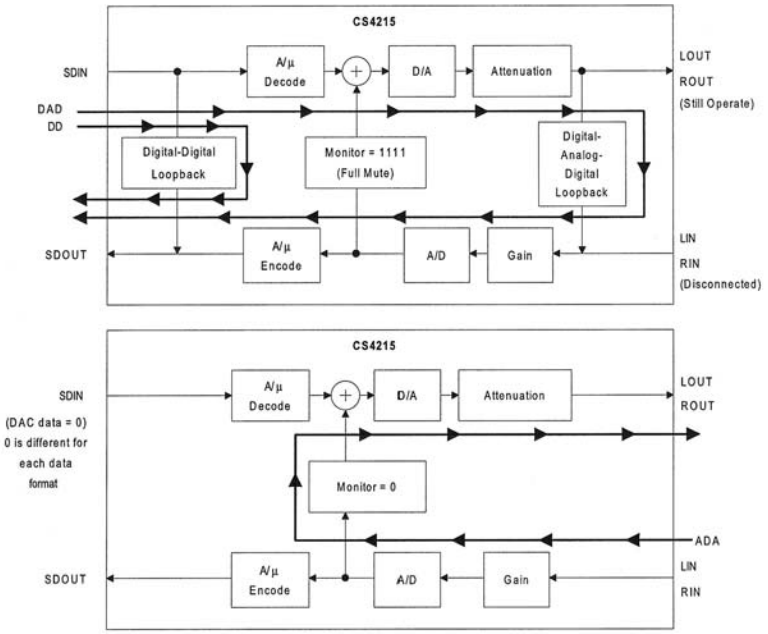

Figure 16. DD, DAD & ADA Loopback Paths

Power Down Mode

Bringing the PDN pin high puts the CS4215 into the power down mode. In this mode HEADC and CMOUT will not supply current. Power down will change all the control registers to the reset state shown under each Control Time Slot register. In the power down mode, the TSOUT pin will follow the TSIN state with less than 10 ns delay.

After returning to normal operation from power down, an offset calibration cycle must be executed. Either bringing $\overline{\text{RESET}}$ low then high, or updating the control registers, will cause an offset calibration cycle. In either case, a delay of 50 ms must occur after PDN goes low before executing the offset calibration. This allows the internal voltage reference time to settle.

LOOPBACK TEST MODES

The CS4215 contains three loopback modes that may be used to test the codec. Two of the loopback test modes are designed to allow the host to perform a self-test on the CS4215. The third mode allows laboratory testing using external equipment.

Host Self-Test Loopback Modes

Since the CS4215 is a mixed-signal device, it is equipped with an internal register that will enable the host to perform a two-tiered test on power-up or as needed. The loopback test is enabled by setting the Enable Loopback bit, ENL, in control register 4. The first tier of loopback is a digital-digital loopback, DD, which is selected by clearing the DAD bit in control register 4 (see

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Figure 16). DD loopback checks the interface between the host and the CS4215 by taking the data on SDIN and looping it back onto SDOUT, with the data on SDOUT being one frame delayed from the data on SDIN. The host can verify that the data received is exactly the same as the data sent, thereby indicating the interface between the two devices and the digital interface on the CS4215 are operating properly. The output DAC's are functional in DD loopback. Now that the interface has been verified, the rest of the CS4215 can be tested using the second tier of loopback.

The second tier of loopback is a digital-analog-digital loopback, DAD, which is selected by setting the DAD bit in control register 4. DAD loopback checks the analog section of the CS4215 by connecting the right and left analog outputs, after the output attenuator, to the analog inputs of the gain stage. This allows testing of most of the CS4215 from the host by sending a known digital signal to the DACs and monitoring the digital signal from the ADCs. During DAD loopback, the monitor attenuator must be set at maximum (full mute), and the analog outputs may be individually muted. The analog inputs are disconnected internally. The flow of test data for both DD and DAD loopback modes is illustrated in the top portion of Figure 16.

Analog-to-Analog Loopback Mode

A third loopback mode is achieved by setting the monitor attenuator to zero attenuation and sending the DACs digital zero via SDIN. This loopback is termed analog-digital-analog, ADA, since the selected analog input will now appear on the enabled analog outputs. Since this test is controlled by external stimulus and the host is not involved (except to send the DACs zeros), it is generally considered a laboratory test as opposed to a self test. The bottom portion of Figure 16 illustrates the ADA signal flow through the CS4215. Note that this test requires the host send analog zeros to the DAC. Each data format has a different code for zero. See Figures 13 and 14.

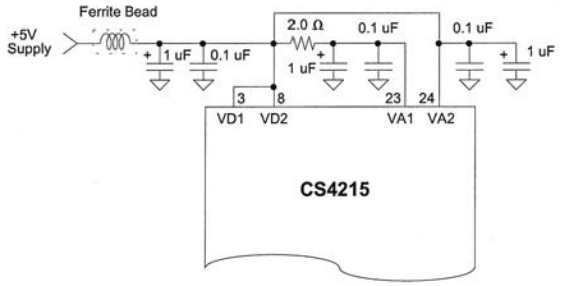

Figure 17. Optional Power Supply Arrangement

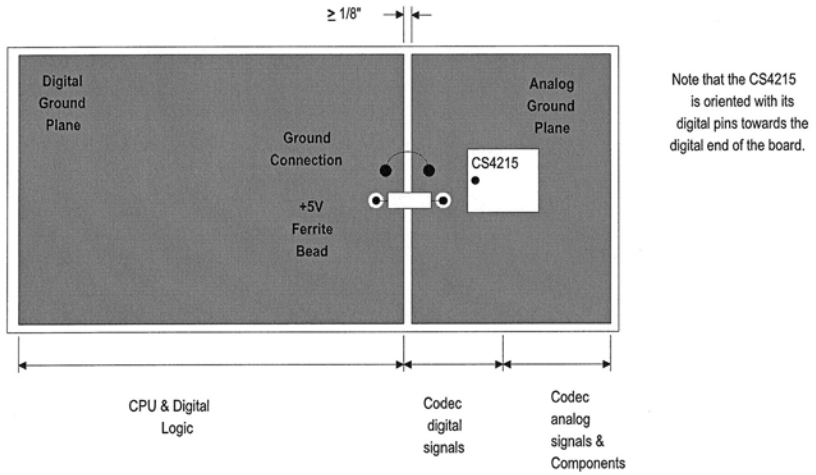

Figure 18. Suggested Layout Guideline

POWER SUPPLY AND GROUNDING

When using separate supplies, the digital power should be connected to the CS4215 via a ferrite bead, positioned closer than 1" to the device (see Figure 1). The codec VA1, VA2 pins should be derived from the cleanest power source available. If only one supply is available, use the suggested arrangement in Figure 17. VA1 supplies analog power to the ADCs and DACs while VA2 supplies power to the output power drivers (headphones and speaker). The large currents necessary for VA2 are not flowing through the 2.0 Ω resistor, and therefore do not corrupt the VA1 converter supply.

The CS4215 along with associated analog circuitry, should be positioned near to the edge of the circuit board, and have its own, separate, ground plane. On the CS4215, the analog and digital grounds are internally connected; therefore, the four ground pins must be externally connected with zero impedance between ground pins. The best solution is to place the entire chip on a solid ground plane as shown in Figure 18. Preferably, it should also have its own power plane. A single connection between the CS4215 ground and the board ground should be positioned as shown in Figure 18.

Figure 19 illustrates the optimum ground and decoupling layout for the CS4215 assuming a surface-mount socket and leaded decoupling capacitors. Surface-mount sockets are useful since the pad locations are exactly the same as the actual chip; therefore, given that space for the socket is left on the board, the socket can be optional for production. Figure 19 depicts the top layer containing signal traces and assumes the bottom or inter-layer contains a solid analog ground plane. The important points with regards to this diagram are that the ground plane is SOLID under the codec and connects all codec ground pins with thick traces providing the absolute lowest impedance between ground pins. The decoupling capacitors are placed as close as possible to the device which, in this case, is the socket boundary. The lowest value capacitor is

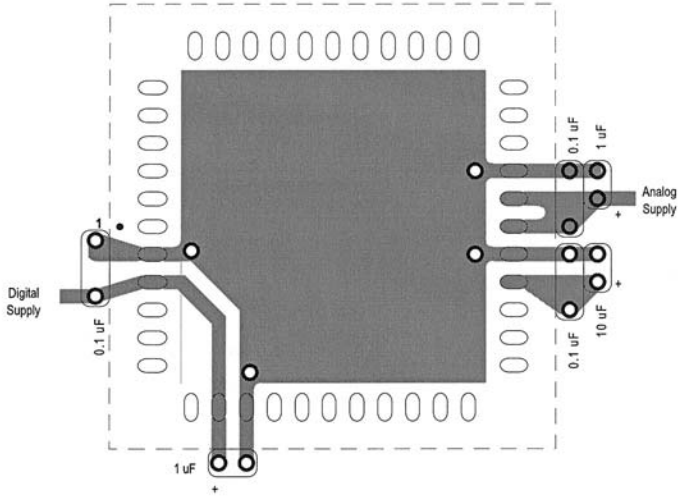

Figure 19. CS4215 Decoupling Layout Guideline

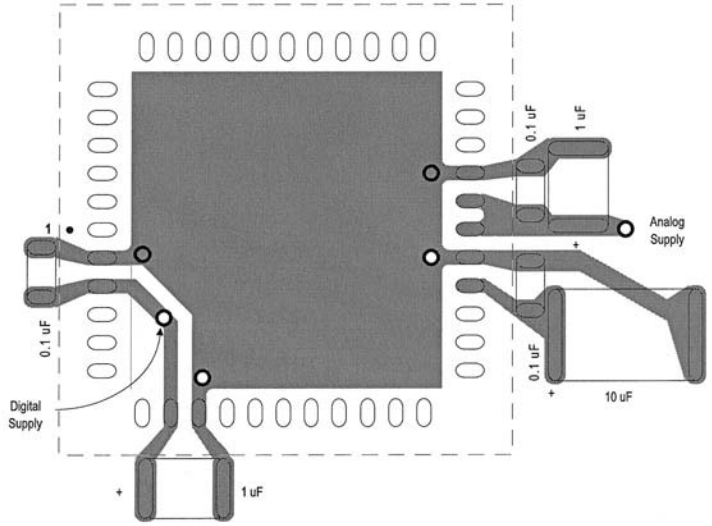

Figure 20. CS4215 Surface Mount Decoupling Layout

placed closest to the codec. Vias are placed near the AGND and DGND pins, under the IC, and should be attached to the solid analog ground plane on another layer. The negative side of the decoupling capacitors should also attach to the same solid ground plane. Traces bringing the power to the codec should be wide thereby keeping the impedance low.

Although not shown in the figures, the trace layers (top layer in the figures) should have ground plane fill in-between the traces to minimize coupling into the analog section. See the CDB4215 evaluation board data sheet for an example layout.

If using all surface-mount components, the decoupling capacitors should still be placed on the layer with the codec and in the positions shown in Figure 20. The vias shown are assumed to attach to the appropriate power and analog ground layers. Traces bringing power to the codec should be as wide as possible to keep the impedance low. For the same reason, vias should be large for power and ground runs.

If using through-hole sockets, effort should be made to find a socket with the minimum height which will minimize the socket impedance. When using a through-hole socket, the vias under the codec in Figure 19 are not needed since the pins serve the same function.

ADC and DAC Filter Response Plots

Figures 21 through 27 show the overall frequency response, passband ripple and transition band for the CS4215 ADCs and DACs. Figure 27 shows the DACs' deviation from linear phase. Fs is the selected sample frequency. Since the sample frequency is programmable, the filters will adjust to the selected sample frequency. Fs is also the FSYNC frequency.

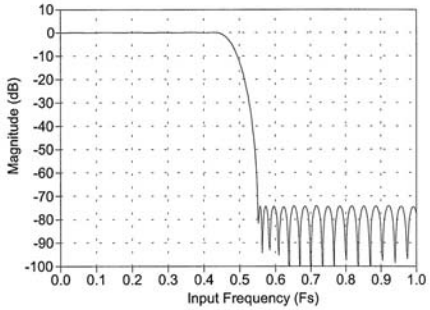

Figure 21. ADC Frequency Response

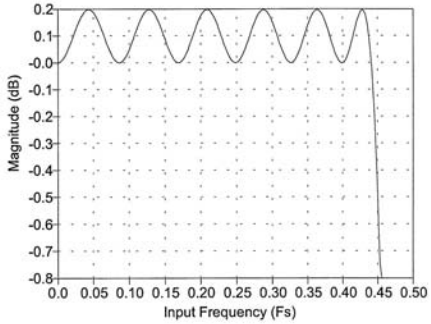

Figure 22. ADC Passband Ripple

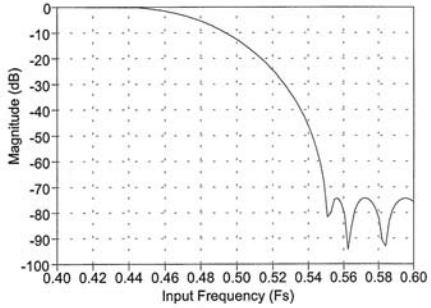

Figure 23. ADC Transition Band

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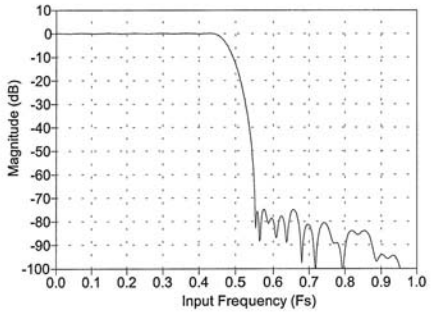


Figure 24. DAC Frequency Response

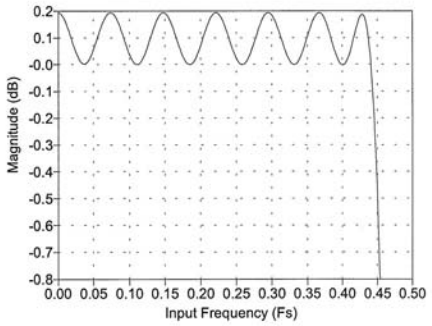


Figure 25. DAC Passband Ripple

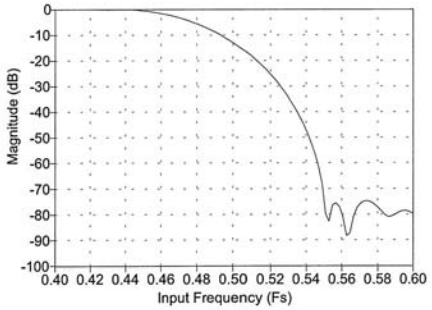


Figure 26. DAC Transition Band

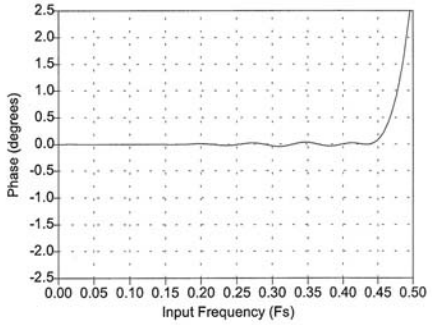
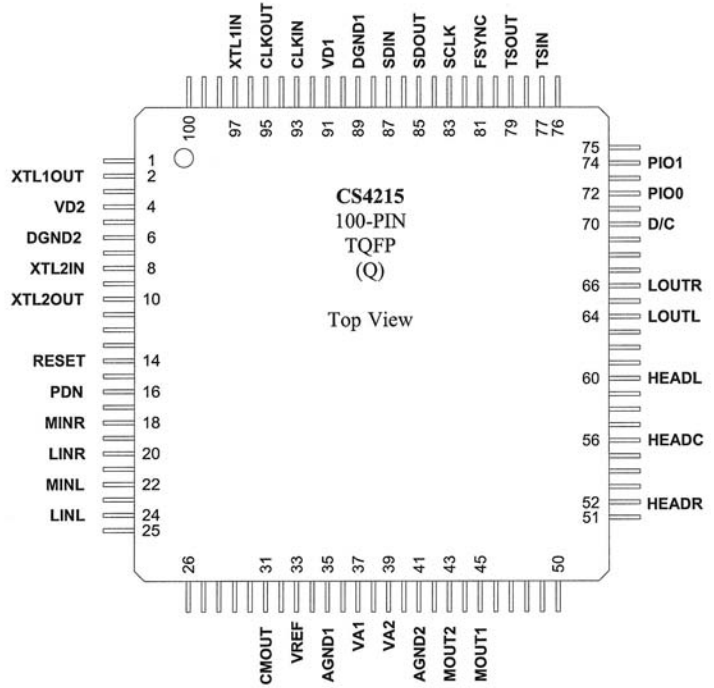
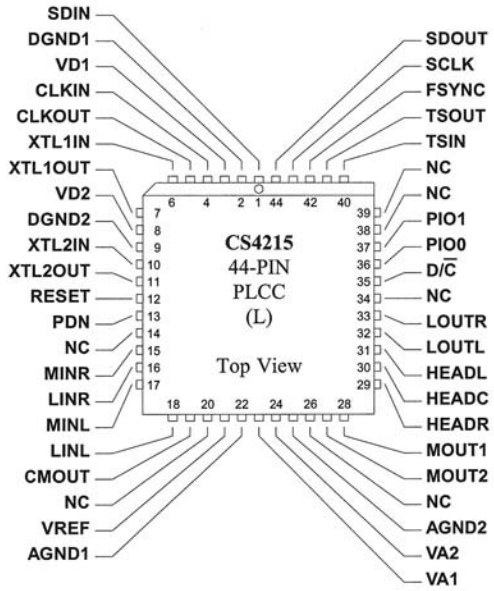


Figure 27. DAC Deviation from Linear Phase

PIN DESCRIPTIONS



Note: All unlabeled pins are No Connects



Power Supply

VA1, VA2 - Analog Power Input, Pins 23(L), 24(L), 37(Q), 39 (Q)
+5 V analog supply.

AGND1, AGND2 - Analog Ground, Pins 22(L), 25(L), 35(Q), 41(Q)
Analog ground. Must be connected to DGND1, DGND2 with zero impedance.

VD1, VD2 - Digital Power Input, Pins 3(L), 8(L), 91(Q), 4(Q)
+ 5 V digital supply.

DGND1, DGND2 - Digital Ground, Pin 2(L), 9(L), 89(Q), 6(Q)
Digital ground. Must be connected to AGND1, AGND2 with zero impedance.

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Analog Inputs

LINL, LINR - Left and Right Channel Line Level Inputs, Pins 18(L), 16(L), 24(Q), 20(Q)
Line level input connections for the right and left channels.

MINL, MINR - Left and Right Channel Microphone Inputs, Pins 17(L), 15(L), 22(Q), 18(Q)
Microphone level input connections for the right and left channels.

Analog Outputs

LOUTR, LOUTL - Line Level Outputs, Pins 33(L), 32(L), 66(Q), 64(Q)
One pair of line level outputs are provided. The output level for right and left outputs can be independently varied. These outputs can be muted.

HEADR, HEADL - Headphone Outputs, Pins 29(L), 31(L), 52(Q), 60(Q)
HEADR and HEADL are intended to drive a pair of headphones. Additional current drive, along with an optional +3 dB of gain, ensures reasonable listening levels. These outputs can be muted.

HEADC - Common Return for Headphone Outputs, Pin 30(L), 56(Q)
HEADC is the return path for large currents when driving headphones from the HEADR and HEADL outputs. This pin is nominally at 2.1 V.

CMOUT - Common Mode Output, Pin 19(L), 31(Q)
Common mode voltage output. This signal may be used for level shifting the analog inputs. The load on CMOUT must be DC only, with an impedance of not less than 10kΩ. CMOUT should be bypassed with a 0.47 µF to AGND. CMOUT is nominally at +2.1V.

MOUT1, MOUT2 - Mono Speaker Outputs, Pins 28(L), 27(L), 45(Q), 43(Q)
Mono external loudspeaker differential output connections. The loudspeaker output is a mix of left and right line outputs. Independent muting of the speaker is provided. MOUT1 and MOUT2 output voltage is nominally at 2.1 V with no signal.

VREF - Voltage Reference Output, Pin 21(L), 33(Q)
The on-chip generated ADC/DAC reference voltage is brought out to this pin for decoupling purposes. This output must be bypassed with a 10 µF capacitor in parallel with a 0.1 µF capacitor to the adjacent AGND1 pin. No other external load may be connected to this output.

Digital Interface Signals

SDIN - Serial Data Input, Pin 1(L), 87(Q)
Audio data for the DACs and control information for all functions is presented to the CS4215 on this pin.

SDOUT - Serial Data Output, Pin 44(L), 85(Q)
Audio data from the ADCs and status information concerning all functions is written out by the CS4215 onto this pin.

SCLK - Serial Port Clock, Pin 43(L), 83(Q)

SCLK rising causes the data on SDOUT to be updated. SCLK falling latches the data on SDIN into the CS4215. The SCLK signal can be generated off-chip, and input into the CS4215. Alternatively, the CS4215 can generate and output SCLK in data mode.

FSYNC - Frame Sync Signal, Pin 42(L), 81(Q)

The Frame Synchronizing Signal is sampled by SCLK, with a rising edge indicating a new frame is about to start. FSYNC frequency is always the system sample rate. Each frame may have 64, 128 or 256 data bits, allowing for 1, 2 or 4 CS4215s connected to the same bus. FSYNC may be input to the CS4215, or may be generated and output by the CS4215 in data mode. When FSYNC is an input, it must be high for at least 1 SCLK period. FSYNC can stay high for the rest of the frame, but must return low at least 2 SCLKs before the next frame starts.

TSIN - Time Slot Input, Pin 40(L), 77(Q)

TSIN high for at least 1 SCLK cycle indicates to the CS4215 that the next time slot is allocated for it to use. TSIN is normally connected to the TSOUT pin of the previous device in the chain. TSIN should be connected to FSYNC for the 1st (or only) CS4215 in the chain.

TSOUT - Time Slot Output, Pin 41(L), 79(Q)

TSOUT goes high for 1 SCLK cycle, indicating that the CS4215 is about to release the data bus. Normally connected to the TSIN pin on the next device in the chain.

D/$\overline{C}$ - Data/Control Select Input, Pin 35(L), 70(Q)

When D/$\overline{C}$ is low, the information on SDIN and SDOUT is control information. When D/$\overline{C}$ is high, the information on SDIN and SDOUT is data information.

PDN - Power Down Input, Pin 13(L), 16(Q)

When high, the PDN pin puts the CS4215 into the power down mode. In this mode HEADC and CMOUT will not supply current. Power down causes all the control registers to change to the default reset state. In the power down mode, the TSOUT pin remains active, and follows TSIN delayed by less than 10 ns.

$\overline{\text{RESET}}$ - Active Low Reset Input, Pin 12(L), 14(Q)

Upon reset, the values of the control information (when D/$\overline{C}$ = 0) will be initialized to the values given in the Reset Description section of this data sheet.

Clock and Crystal Pins

XTL1IN, XTL1OUT, XTL2IN, XTL2OUT - Crystals 1 and 2 Inputs and Outputs, Pins 6(L), 7(L), 10(L), 11(L), 97(Q), 2(Q), 8(Q), 10(Q)

Input and output connections for crystals 1 and 2. One of these oscillators may provide the master clock to run the CS4215.

CLKIN - External Clock Input, Pin 4(L), 93(Q)

External clock input optionally used to clock the CS4215. The CLKIN frequency must be 256 times the maximum sample rate (FSYNC frequency).

CLKOUT - Master Clock Output, Pin 5(L), 95(Q)

Master clock output, whose frequency is always 256 times the system sample rate (FSYNC frequency). CLKOUT is active only in data mode and is low during control mode.

Miscellaneous Pins

PIO0, PIO1 - Parallel Input/Output, Pins 36(L), 37(L), 72(Q), 74(Q)

These pins are provided as general purpose digital parallel input/output and have open drain outputs. An external pull-up resistor is required. They can be read in control mode, and read and written to in data mode.

Note: All unlabeled pins are No Connects which should be left floating.

PARAMETER DEFINITIONS

Resolution

The number of bits in the input words to the DACs, and in the output words in the ADCs.

Differential Nonlinearity

The worst case deviation from the ideal codewidth. Units in LSB.

Total Dynamic Range

The rms value of a full scale signal to the lowest obtainable noise floor. It is measured by comparing a full scale signal to the lowest noise floor possible in the codec (ie. attenuation bits for the DACs at full attenuation.) Units in dB.

Instantaneous Dynamic Range

The dynamic range available at any instant in time. It is measured using S/(N+D) with a 1 kHz, -60 dB input signal, with 60 dB added to compensate for the small input signal. Use of a small input signal reduces to harmonic distortion components of the noise to insignificance. Units in dB.

Total Harmonic Distortion

THD is the ratio of the rms value of a signal's first five harmonic components to the rms value of the signals fundamental component. THD is calculated for the ADCs using an input signal which is 3dB below typical full-scale, and is referenced to typical full-scale. A digital full-scale output is used to calculate THD for the DACs.

Interchannel Isolation

The amount of 1 kHz signal present on the output of the grounded input channel with 1 kHz 0 dB signal present on the other channel. Units in dB.

Interchannel Gain Mismatch

For the ADCs, the difference in input voltage that generates the full scale code for each channel. For the DACs, the difference in output voltages for each channel with a full scale digital input. Units in dB.

Frequency Response

Worst case variation in output signal level versus frequency over 10 Hz to 20 kHz. Units in dB.

Step Size

Typical delta between two adjacent gain or attenuation values. Units in dB.

Absolute Step Error

The deviation of a gain or attenuation step from a straight line passing through the no-gain/attenuation value and the full-gain/attenuation value (i.e. end points). Units in dB.

Out-of-Band Energy

The ratio of the rms sum of the energy from 0.46xFs to 2.1xFs compared to the rms full-scale signal value. Tested with 48kHz Fs giving an out-of-band energy range of 22kHz to 100kHz.

Offset Error

For the ADCs, the deviation in LSBs of the output from mid-scale with the selected input at CMOUT. For the DACs, the deviation of the output from CMOUT with mid-scale input code. Units in volts.