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HEWLETT PACKARD

Cascadable Silicon Bipolar MMIC Amplifier

Technical Data

MSA-1105

Features

- **High Dynamic Range Cascadable 50 Ω or 75 Ω Gain Block**
- **3 dB Bandwidth:** 50 MHz to 1.3 GHz
- **17.5 dBm Typical $P_{1\ dB}$ at 0.5 GHz**
- **3.6 dB Typical Noise Figure at 0.5 GHz**
- **Surface Mount Plastic Package**
- **Tape-and-Reel Packaging Option Available**[1]

Note:

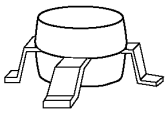
1. Refer to PACKAGING section "Tape-and-Reel Packaging for Semiconductor Devices."

Description

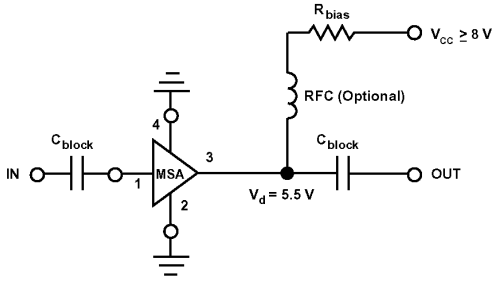
The MSA-1105 is a high performance silicon bipolar Monolithic Microwave Integrated Circuit (MMIC) housed in a low cost, surface mount plastic package. This MMIC is designed for high dynamic range in either 50 or 75 Ω systems by combining low noise figure with high IP_3. Typical applications include narrow and broadband linear amplifiers in commercial and industrial systems.

The MSA-series is fabricated using HP's 10 GHz f_T, 25 GHz f_{MAX} silicon bipolar MMIC process which uses nitride self-alignment, ion implantation, and gold metallization to achieve excellent performance, uniformity and reliability. The use of an external bias resistor for temperature and current stability also allows bias flexibility.

05 Plastic Package



Typical Biasing Configuration



MSA-1105 Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Current	80 mA
Power Dissipation[2,3]	550 mW
RF Input Power	+13dBm
Junction Temperature	150°C
Storage Temperature	–65 to 150°C

Thermal Resistance[2,4]:
$\theta_{jc} = 125°C/W$

Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. $T_{CASE} = 25°C$.
3. Derate at 8 mW/°C for $T_C > 124°C$.
4. See MEASUREMENTS section "Thermal Resistance" for more information.

Electrical Specifications[1], $T_A = 25°C$

Symbol	Parameters and Test Conditions: $I_d = 60$ mA, $Z_O = 50\ \Omega$		Units	Min.	Typ.	Max.
G_P	Power Gain ($\|S_{21}\|^2$)	f = 0.05 GHz f = 0.5 GHz f = 1.0 GHz	dB dB dB	 10.0	12.7 12.0 10.5	
ΔG_P	Gain Flatness	f = 0.1 to 1.0 GHz	dB		± 1.0	
$f_{3\ dB}$	3 dB Bandwidth[2]		GHz		1.3	
VSWR	Input VSWR	f = 0.1 to 1.0 GHz			1.5:1	
	Output VSWR	f = 0.1 to 1.0 GHz			1.7:1	
NF	50 Ω Noise Figure	f = 0.5 GHz	dB		3.6	
$P_{1\ dB}$	Output Power at 1 dB Gain Compression	f = 0.5 GHz	dBm		17.5	
IP_3	Third Order Intercept Point	f = 0.5 GHz	dBm		30.0	
t_D	Group Delay	f = 0.5 GHz	psec		200	
V_d	Device Voltage		V	4.4	5.5	6.6
dV/dT	Device Voltage Temperature Coefficient		mV/°C		–8.0	

Notes:
1. The recommended operating current range for this device is 40 to 70 mA. Typical performance as a function of current is on the following page.
2. Referenced from 50 MHz gain (G_P).

Part Number Ordering Information

Part Number	No. of Devices	Container
MSA-1105-TR1	500	7" Reel
MSA-1105-STR	10	Antistatic Bag

For more information, see "Tape and Reel Packaging for Semiconductor Devices".

MSA-1105 Typical Scattering Parameters (Z_O = 50 Ω, T_A = 25°C, I_d = 60 mA)

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}		k
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang	
.0005	.30	–17	19.0	8.94	171	–26.0	.050	51	.31	–16	0.53
.005	.26	–62	13.9	4.98	163	–16.8	.144	15	.26	–64	0.93
.025	.07	–48	12.8	4.36	174	–16.4	.151	4	.08	–52	1.08
.050	.06	–38	12.7	4.33	174	–16.3	.153	2	.06	–48	1.08
.100	.05	–41	12.7	4.31	170	–16.4	.152	3	.06	–52	1.09
.200	.06	–58	12.6	4.26	162	–16.2	.155	5	.08	–73	1.08
.300	.07	–74	12.4	4.19	154	–16.1	.157	7	.10	–91	1.07
.400	.09	–91	12.2	4.10	146	–15.8	.163	8	.12	–105	1.06
.500	.10	–105	12.0	4.00	138	–15.6	.166	8	.14	–116	1.05
.600	.11	–116	11.8	3.88	131	–15.4	.171	10	.17	–126	1.04
.700	.13	–128	11.5	3.76	123	–15.0	.178	11	.18	–135	1.03
.800	.15	–136	11.2	3.63	116	–14.7	.184	11	.21	–144	1.01
.900	.16	–145	10.9	3.49	109	–15.5	.188	11	.22	–151	1.01
1.000	.18	–152	10.5	3.37	102	–14.1	.197	11	.24	–159	1.00
1.500	.28	174	8.8	2.75	72	–13.2	.219	7	.31	170	1.00
2.000	.38	150	7.1	2.28	48	–12.1	.248	0	.34	151	0.99
2.500	.46	133	5.6	1.90	28	–11.9	.254	–4	.38	134	1.02
3.000	.53	118	4.2	1.62	11	–11.6	.262	–8	.40	122	1.04

A model for this device is available in the DEVICE MODELS section.

Typical Performance, T_A = 25°C, Z_O = 50 Ω

(unless otherwise noted)

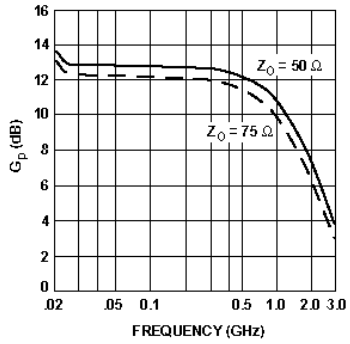


Figure 1. Typical Power Gain vs. Frequency, I_d = 60 mA.

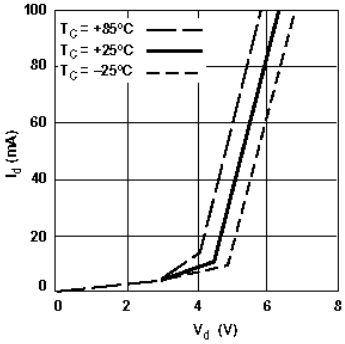


Figure 2. Device Current vs. Voltage.

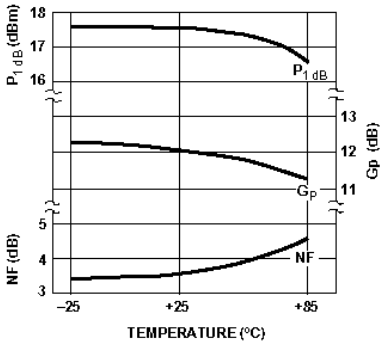


Figure 3. Output Power at 1 dB Gain Compression, Noise Figure and Power Gain vs. Case Temperature, f = 0.5 GHz, I_d = 60 mA.

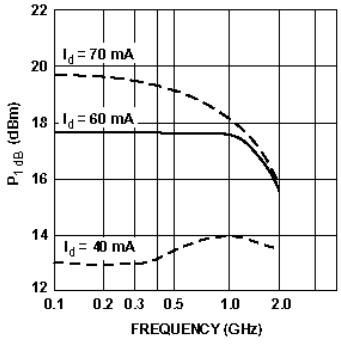


Figure 4. Output Power at 1 dB Gain Compression vs. Frequency.

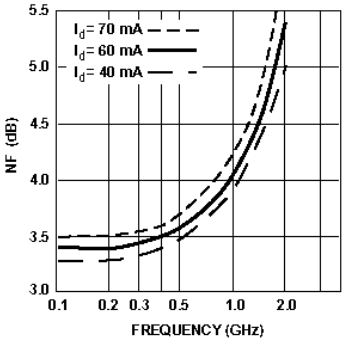


Figure 5. Noise Figure vs. Frequency.

Agilent Technologies

Surface Mount RF PIN Diodes

Technical Data

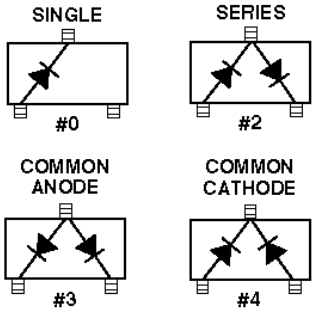
HSMP-383x Series

Features

- **Diodes Optimized for:**
  Low Capacitance Switching
  Low Current Attenuator
- **Surface Mount SOT-23 Package**
  Single and Dual Versions
  Tape and Reel Options Available
- **Low Failure in Time (FIT) Rate**[1]
- **Lead-free Option Available**

Note:
1. For more information see the Surface Mount PIN Reliability Data Sheet.

Package Lead Code Identification (Top View)



Description/Applications

The HSMP-383x series of general purpose PIN diodes are designed for two classes of applications. The first is attenuators where current consumption is the most important design consideration. The second application for this series of diodes is in switches where low capacitance is the driving issue for the designer.

The HSMP-386x series Total Capacitance (C_T) and Total Resistance (R_T) are typical specifications. For applications that require guaranteed performance, the general purpose HSMP-383x series is recommended.

A SPICE model is not available for PIN diodes as SPICE does not provide for a key PIN diode characteristic, carrier lifetime.

Absolute Maximum Ratings[1] T_C = 25°C

Symbol	Parameter	Units	Absolute Maximum
I_f	Forward Current (1 ms Pulse)	Amp	1
P_t	Total Device Dissipation	mW[2]	250
P_{iv}	Peak Inverse Voltage	—	Same as V_{BR}
T_j	Junction Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to 150

Notes:
1. Operation in excess of any one of these conditions may result in permanent damage to this device.
2. CW Power Dissipation at T_{LEAD} = 25°C. Derate to zero at maximum rated temperature.

PIN General Purpose Diodes, Electrical Specifications T_C = 25°C

Part Number HSMP-	Package Marking Code[1]	Lead Code	Configuration	Minimum Breakdown Voltage V_{BR} (V)	Maximum Series Resistance R_S (Ω)	Maximum Total Capacitance C_T (pF)
3830 3832 3833 3834	K0 K2 K3 K4	0 2 3 4	Single Series Common Anode Common Cathode	200	1.5	0.3
Test Conditions				$V_R = V_{BR}$ Measure $I_R \leq 10$ mA	I_F = 100 mA f = 100 MHz	V_R = 50 V f = 1 MHz

Typical Parameters at T_C = 25°C

Part Number HSMP-	Series Resistance R_S (Ω)	Carrier Lifetime τ (ns)	Reverse Recovery Time T_{rr} (ns)	Total Capacitance C_T (pF)
383x	20	500	80	0.20 @ 50 V
Test Conditions	I_F = 1 mA f = 100 MHz	I_F = 50 mA I_R = 250 mA	V_R = 10 V I_F = 20 mA 90% Recovery	

Note:
1. Package marking code is white.

Typical Parameters at T_C = 25°C (unless otherwise noted), Single Diode

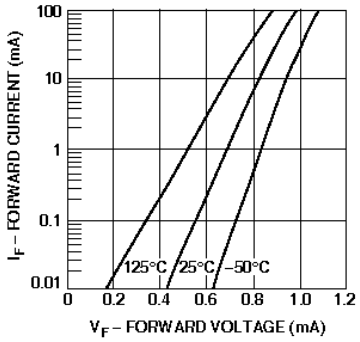


Figure 1. Forward Current vs. Forward Voltage.

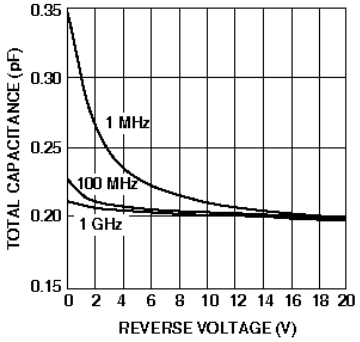


Figure 2. RF Capacitance vs. Reverse Bias.

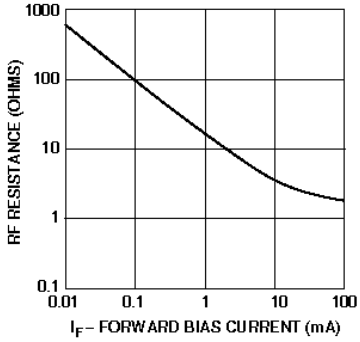


Figure 3. RF Resistance at 25°C vs. Forward Bias Current.

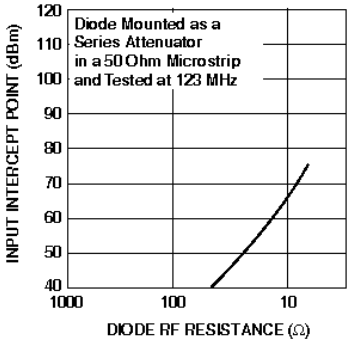


Figure 4. 2nd Harmonic Input Intercept Point vs. Diode RF Resistance for Attenuators.

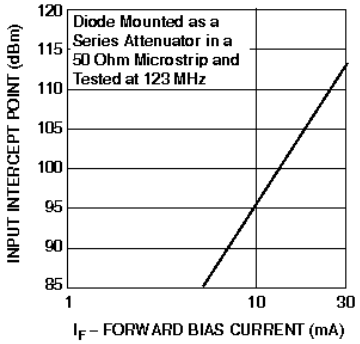


Figure 5. 2nd Harmonic Input Intercept Point vs. Forward Bias Current for Switches.

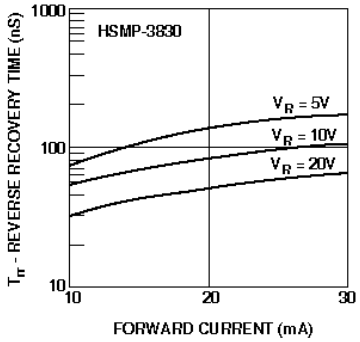


Figure 6. Reverse Recovery Time vs. Forward Current for Various Reverse Voltage.

JENNINGS TECHNOLOGY

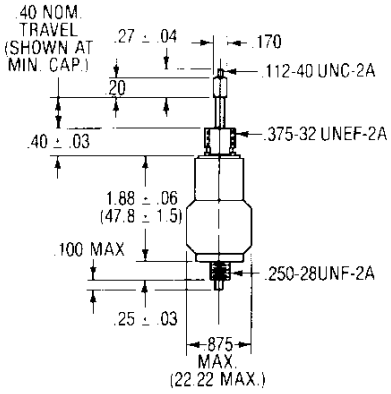
Gas Variable Capacitors
CHV1 45

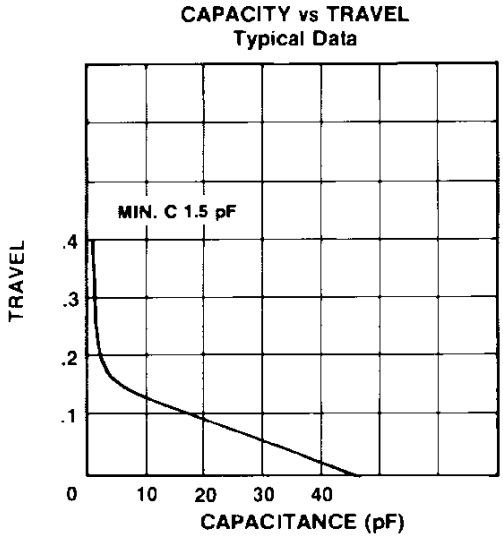
CHV1 45 SPECIFICATIONS

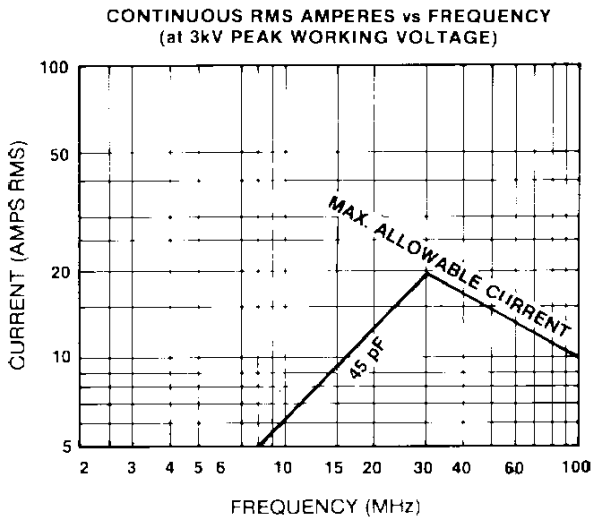
Model Number	CHV1-45-0103*	CHV1-45-0105*	CHV1-45-0107*
Capacity Range (pF)	1.5-45	1.5-45	1.5-45
Voltage (kV) Peak			
Test	3.0	5.0	7.5
Working	1.8	3.0	4.5
Current Amps (RMS) Max.	13	18	20
Type	Ceramic	Ceramic	Ceramic
Nominal Dimensions			
Length (in. / mm)	3.50 / 88.90	3.50 / 88.90	3.50 / 88.90
Diameter (in. / mm)	0.88 / 22.20	0.88 / 22.20	0.88 / 22.20
Torque (in Lbs.) Max.	N/A	N/A	N/A
Push Force @ 25°C	20 lb.	20 lb.	20 lb.
Weight (Nominal)	3 oz.	3 oz.	3 oz.

NOTES:
Mounting: Fixed and variable end threaded.

* CHV1N (non-magnetic version) available.







Jennings Technology Company • 970 Mc Laughlin Avenue, San Jose CA 95122 • Tel: (408) 292-4025 • Fax: (408) 286-1789 • Web: http://www.jenningstech.com

UHF push-pull power MOS transistor BLF548

FEATURES

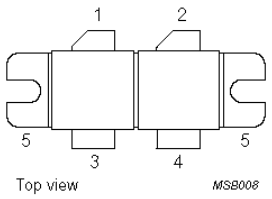
- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability
- Designed for broadband operation.

DESCRIPTION

Dual push-pull silicon N-channel enhancement mode vertical D-MOS transistor designed for communications transmitter applications in the UHF frequency range.

The transistor is encapsulated in a 4-lead, SOT262A2 balanced flange package, with two ceramic caps. The mounting flange provides the common source connection for the transistors.

PIN CONFIGURATION



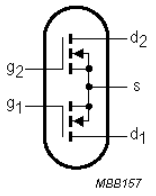


Fig.1 Simplified outline and symbol.

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A, and SNW-FQ-302B.

PINNING - SOT262A2

PIN	DESCRIPTION
1	drain 1
2	drain 2
3	gate 1
4	gate 2
5	source

WARNING

Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a push-pull common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	500	28	150	>10	>50

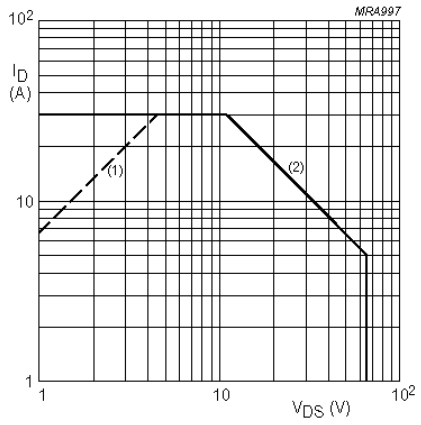
LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor section unless otherwise specified					
V_{DS}	drain-source voltage		–	65	V
V_{GS}	gate-source voltage		–	±20	V
I_D	drain current (DC)		–	15	A
P_{tot}	total power dissipation	$T_{mb} \leq 25$ °C; total device; both sections equally loaded	–	330	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	200	°C

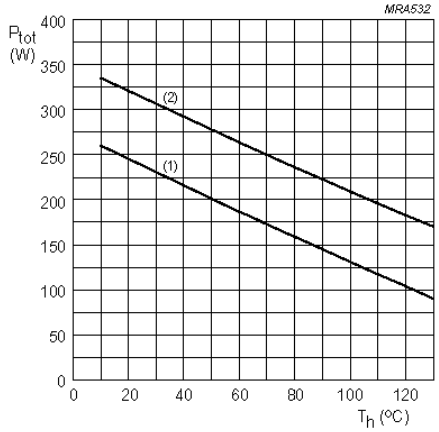
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	T_{mb} = 25 °C; P_{tot} = 330 W; total device; both sections equally loaded	0.5	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	total device; both sections equally loaded	0.15	K/W



(1) Current in this area may be limited by R_{DSon}.
(2) T_{mb} = 25 °C.
Total device; both sections equally loaded.

Fig.2 DC SOAR.



(1) Continuous operation.
(2) Short-time operation during mismatch.
Total device; both sections equally loaded.

Fig.3 Power derating curves.

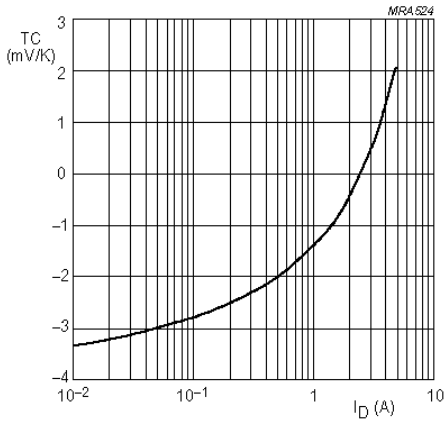
CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per transistor section						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 40 mA	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	0.5	mA
I_{GSS}	gate-source leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	1	µA
V_{GSth}	gate-source threshold voltage	I_D = 160 mA; V_{DS} = 10 V	2	–	4	V
g_{fs}	forward transconductance	I_D = 4.8 A; V_{DS} = 10 V	2.4	3.5	–	S
R_{DSon}	drain-source on-state resistance	I_D = 4.8 A; V_{GS} = 10 V	–	0.25	0.3	Ω
I_{DSX}	on-state drain current	V_{GS} = 15 V; V_{DS} = 10 V	16	20	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	105	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	90	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	25	–	pF

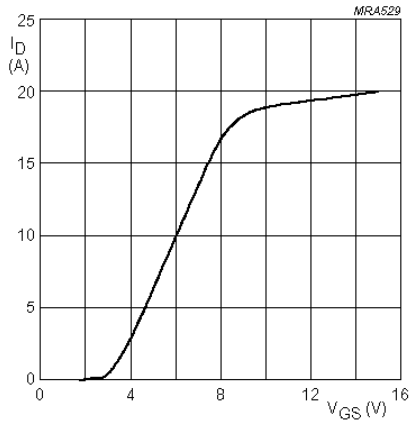
V_{GS} group indicator

GROUP	LIMITS (V)		GROUP	LIMITS (V)	
	MIN.	MAX.		MIN.	MAX.
A	2.0	2.1	O	3.3	3.4
B	2.1	2.2	P	3.4	3.5
C	2.2	2.3	Q	3.5	3.6
D	2.3	2.4	R	3.6	3.7
E	2.4	2.5	S	3.7	3.8
F	2.5	2.6	T	3.8	3.9
G	2.6	2.7	U	3.9	4.0
H	2.7	2.8	V	4.0	4.1
J	2.8	2.9	W	4.1	4.2
K	2.9	3.0	X	4.2	4.3
L	3.0	3.1	Y	4.3	4.4
M	3.1	3.2	Z	4.4	4.5
N	3.2	3.3			



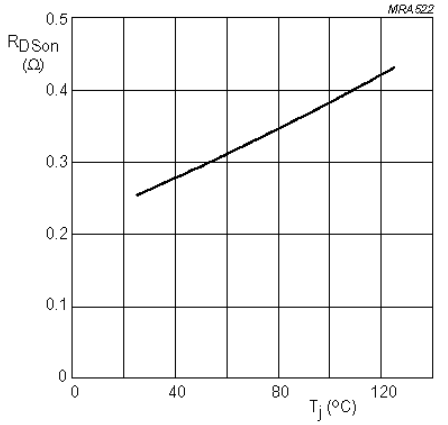
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current; typical values per section.



V_{DS} = 10 V; T_j = 25 °C.

Fig.5 Drain current as a function of gate-source voltage; typical values per section.



I_D = 4.8 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature; typical values per section.

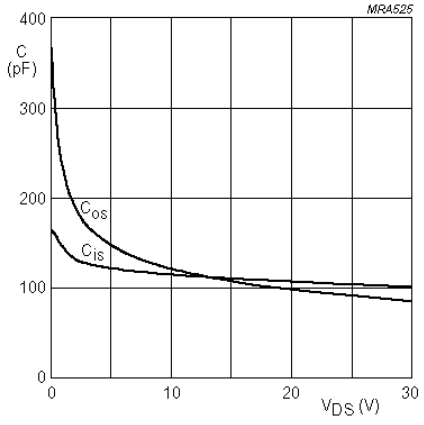


Fig.7 Input and output capacitance as functions of drain-source voltage; typical values per section.

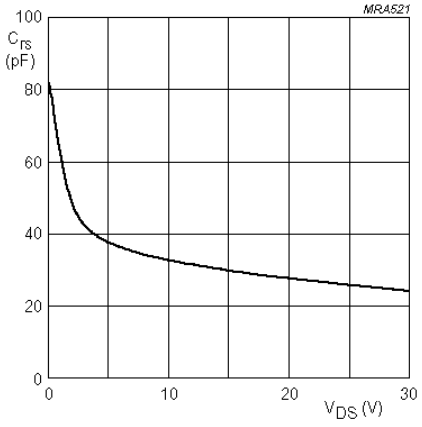


Fig.8 Feedback capacitance as a function of drain-source voltage; typical values per section.

APPLICATION INFORMATION FOR CLASS-B OPERATION

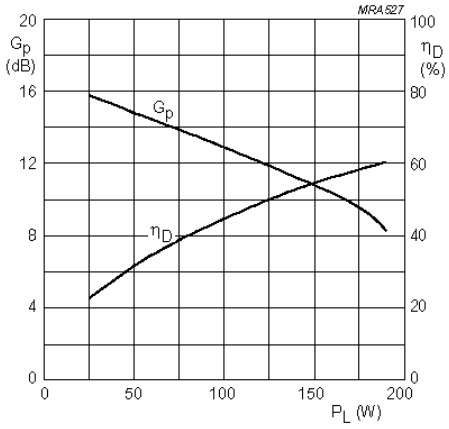
T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.15 K/W, unless otherwise specified.

RF performance in a common source, class-B, push-pull test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	500	28	2 x 160	150	>10 typ. 11	>50 typ. 55

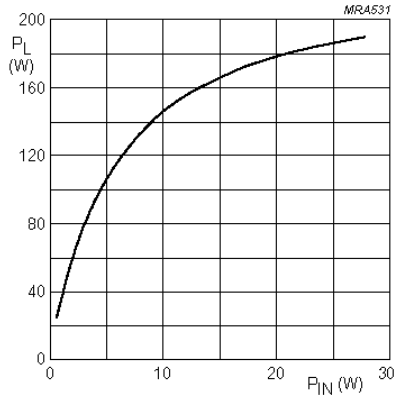
Ruggedness in class-B operation

The BLF548 is capable of withstanding a load mismatch corresponding to VSWR = 10: 1 through all phases under the following conditions: V_{DS} = 28 V; f = 500 MHz at rated output power.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 × 160 mA;
f = 500 MHz; Z_L = 1.1 + j0.6 Ω (per section).

Fig.9 Power gain and efficiency as functions of load power; typical values.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 2 × 160 mA;
f = 500 MHz; Z_L = 1.1 + j0.6 Ω (per section).

Fig.10 Load power as a function of input power; typical values.

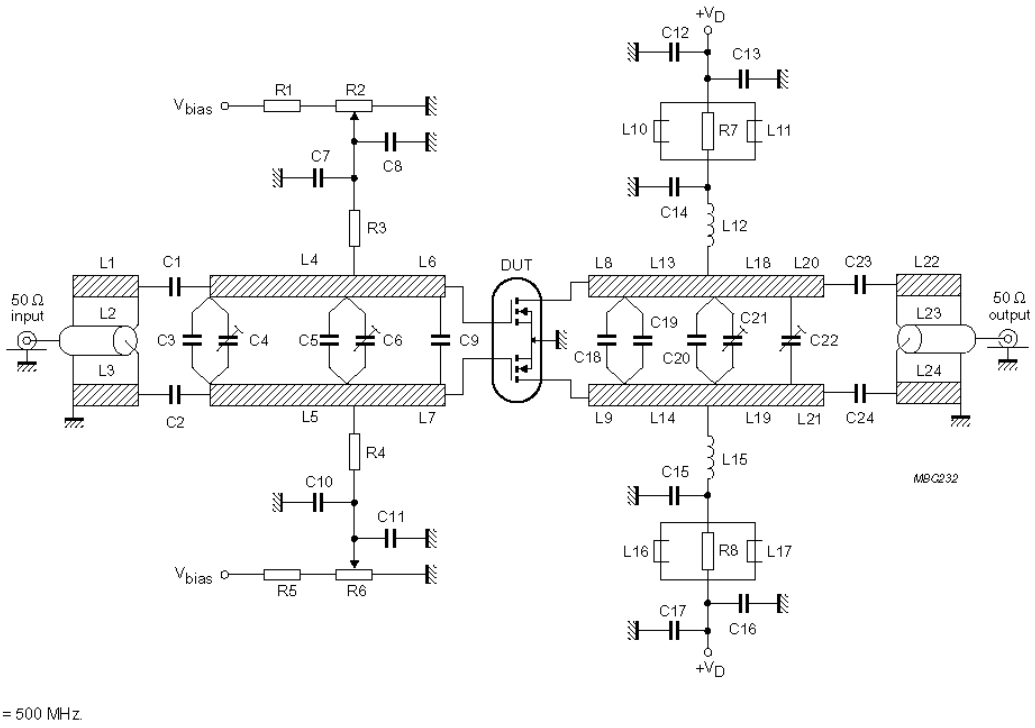
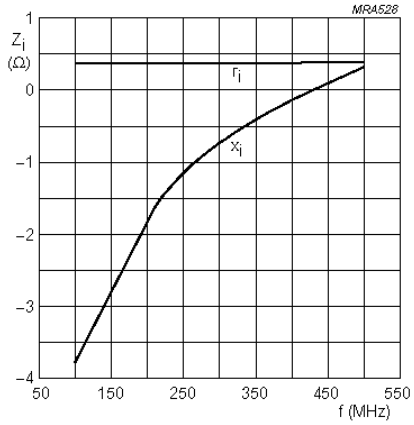


Fig.11 Test circuit for class-B operation.

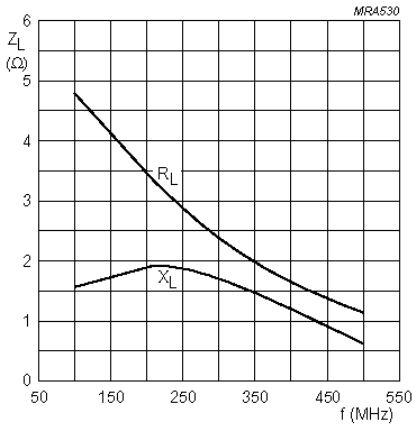
List of components class-B test circuit (see Fig.11)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor; note 1	22 pF		
C3	multilayer ceramic chip capacitor; note 1	16 pF		
C4	film dielectric trimmer	2 to 9 pF		2222 809 09005
C5	multilayer ceramic chip capacitor; note 2	27 pF		
C6, C21, C22	film dielectric trimmer	2 to 18 pF		2222 809 09006
C7, C10, C14, C15	multilayer ceramic chip capacitor; note 1	390 pF		
C8, C11, C12, C17	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C9	multilayer ceramic chip capacitor; note 3	2 × 56 pF in series		



Class-B operation; V_{DS} = 28 V; I_{DQ} = 160 mA (per section); P_L = 150 W (total device).

Fig.13 Input impedance as a function of frequency (series components); typical values per section.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 160 mA (per section); P_L = 150 W (total device).

Fig.14 Load impedance as a function of frequency (series components); typical values per section.

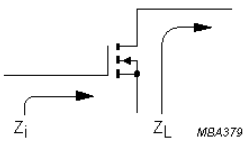
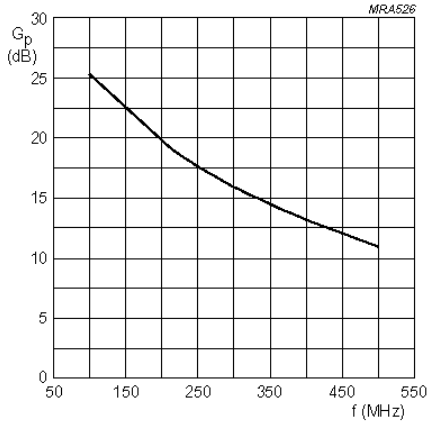


Fig.15 Definition of MOS impedance.



Class-B operation; V_{DS} = 28 V; I_{DQ} = 160 mA (per section); P_L = 150 W (total device).

Fig.16 Power gain as a function of frequency; typical values per section.

Mini-Circuits®

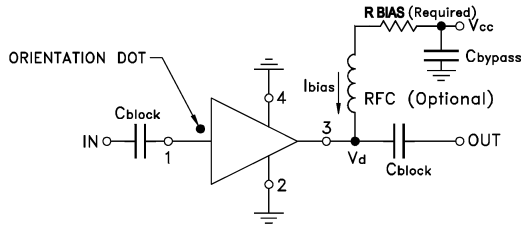
Drop-In & Surface Mount

medium power, up to +18.4 dBm output

all specifications at 25°C

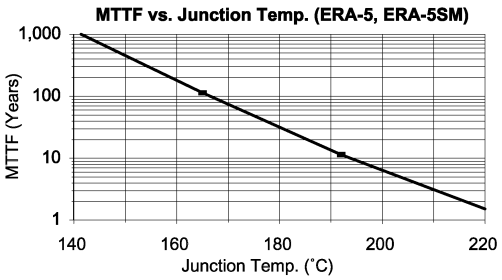
MODEL◆ NO.	✪ FREQ. GHz f_L - f_U	GAIN, dB Typical over frequency, GHz 0.1	1	2	3	4	6	8	Flatness Min.@ 2 GHz	Flatness DC-2 GHz	MAXIMUM POWER (dBm) at 2 GHz* Output (1 dB Comp.) Typ.	Output (1 dB Comp.) Min.	Input (no dmg)	DYNAMIC RANGE at 2 GHz* NF (dB) Typ.	IP3 (dBm) Typ.	VSWR (:1) Typ. In DC-3 GHz	In 3-f_U** GHz	Out DC-3 GHz	Out 3-f_U** GHz	ABSOLUTE MAX. RATING[3] I (mA)	P (mW)	DC OPERATING POWER[4] at Pin 3 Current (mA)	Volt. Typ	Volt. Min	Volt. Max	THERMAL RESISTANCE θjc Typ. °C/W	CASE STYLE Note B	CONNECTION	PRICE $ Qty. (30)
ERA-6	DC-4	12.6	12.5	12.2	11.7	11.3	—	—	10.5	±0.2	17.9	16	20	4.5	36	1.3	1.2	1.6	1.8	120	650	70	5.0	4.6	5.6	170	VV105	cb	3.85
ERA-4	DC-4	14.3	14.0	13.4	12.7	11.8	—	—	11	±0.4	17.3	15	20	4.2	34	1.2	1.2	1.3	1.8	120	650	65	4.5	4.2	5.5	163	VV105	cb	3.85
ERA-5	DC-4	20.2	19.5	18.5	17.3	16.2	—	—	16	±1.0	18.4	16.5	13	4.3	32.5	1.3	1.3	1.2	1.3	120	650	65	4.9	4.2	5.5	278	VV105	cb	3.85
ERA-6SM	DC-4	12.6	12.5	12.2	11.7	11.3	—	—	10.5	±0.2	17.9	16	20	4.5	36	1.3	1.2	1.6	1.8	120	650	70	5.0	4.6	5.6	175	WW107	cb	3.90
ERA-4SM	DC-4	14.3	14.0	13.4	12.7	11.8	—	—	11	±0.4	17.3	15	20	4.2	34	1.2	1.2	1.3	1.8	120	650	65	4.5	4.2	5.5	168	WW107	cb	3.90
NEW ERA-51SM	DC-4	18.0	17.4	16.1	14.8	12.5	—	—	14	±1.0	18.1	16.5	13	4.1	33	1.1	1.2	1.2	1.9	120	650	65	4.5	4.2	5.5	154	WW107	cb	3.90
ERA-5SM	DC-4	20.2	19.5	18.5	17.3	16.2	—	—	16	±1.0	18.4	16.5	13	4.3	32.5	1.3	1.3	1.2	1.3	120	650	65	4.9	4.2	5.5	283	WW107	cb	3.90
NEW ERA-50SM***	DC-1.5	20.7	19.4	18.3	—	—	—	—	16	±1.2	17.2	16.0	13	3.5	32.5	1.3	—	1.2	—	120	650	60	4.4	4.0	4.9	177	WW107	cb	2.95

typical biasing configuration



R BIAS
"1%" Resistor Values (ohms) for Optimum Biasing of ERA Models

Vcc	ERA-1, 1SM	ERA-2, 2SM	ERA-21SM	ERA-3, 3SM	ERA-33SM	ERA-4, 4SM	ERA-5, 5SM	ERA-50SM, 51SM	ERA-6, 6SM
7	90.9	88.7	88.7	107	69.8	38.3	40.2	40.2	30.1
8	113	113	113	133	93.1	52.3	53.6	53.6	43.2
9	137	137	137	162	115	66.5	68.1	68.1	56.2
10	162	162	162	191	140	80.6	82.5	82.5	69.8
11	187	187	187	221	165	95.3	97.6	97.6	84.5
12	215	215	210	249	191	110	113	113	97.6
13	237	237	237	280	215	127	127	127	113
14	261	261	261	309	243	143	143	143	127
15	287	287	287	340	267	158	158	158	140
16	309	316	316	365	287	174	174	174	154
17	332	340	340	392	316	187	191	191	169
18	357	365	365	422	340	205	205	205	182
19	383	392	392	453	365	221	221	221	196
20	412	412	412	475	392	237	237	237	210



designers kits available

KIT NO.	Model Type	No. of Units in Kit	Description	Price $ per kit
K1-ERA	ERA	30	10 of each 1,2,3	49.95
K2-ERA	ERA	20	10 of each 4,5	69.95
K1-ERASM	ERA-SM	30	10 of each 1SM, 2SM,3SM	49.95
K2-ERASM	ERA-SM	20	10 of each 4SM, 5SM	69.95
K3-ERASM	ERA-SM	30	10 of each 4SM, 5SM, 6SM	99.95

pin connections

PORT	cb
RF IN	1
RF OUT	3
DC	3
CASE GND	2,4
NOT USED	—

NSN GUIDE

MCL NO.	NSN
ERA-1SM	5962-01-459-9075
ERA-2SM	5962-01-459-7410
ERA-3SM	5962-01-459-9314

010621

TelCom Semiconductor, Inc.

TC4426
TC4427
TC4428

1.5A DUAL HIGH-SPEED, POWER MOSFET DRIVERS

FEATURES

- **High Peak Output Current 1.5A**
- **Wide Operating Range .....4.5V to 18V**
- **High Capacitive Load Drive Capability ..... 1000 pF in 25 nsec**
- **Short Delay Time ..... <40nsec Typ**
- **Consistent Delay Times With Changes in Supply Voltage**
- **Low Supply Current**
  - **— With Logic "1" Input 4mA**
  - **— With Logic "0" Input 400µA**
- **Low Output Impedance 7Ω**
- **Latch-Up Protected: Will Withstand >0.5A Reverse Current..... Down to – 5V**
- **Input Will Withstand Negative Inputs**
- **ESD Protected.....4kV**
- **Pinout Same as TC426/TC427/TC428**

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC4426COA	8-Pin SOIC	0°C to +70°C
TC4426CPA	8-Pin Plastic DIP	0°C to +70°C
TC4426EOA	8-Pin SOIC	– 40°C to +85°C
TC4426EPA	8-Pin Plastic DIP	– 40°C to +85°C
TC4426MJA	8-Pin CerDIP	– 55°C to +125°C
TC4427COA	8-Pin SOIC	0°C to +70°C
TC4427CPA	8-Pin Plastic DIP	0°C to +70°C
TC4427EOA	8-Pin SOIC	– 40°C to +85°C
TC4427EPA	8-Pin Plastic DIP	– 40°C to +85°C
TC4427MJA	8-Pin CerDIP	– 55°C to +125°C
TC4428COA	8-Pin SOIC	0°C to +70°C
TC4428CPA	8-Pin Plastic DIP	0°C to +70°C
TC4428EOA	8-Pin SOIC	– 40°C to +85°C
TC4428EPA	8-Pin Plastic DIP	– 40°C to +85°C
TC4428MJA	8-Pin CerDIP	– 55°C to +125°C

GENERAL DESCRIPTION

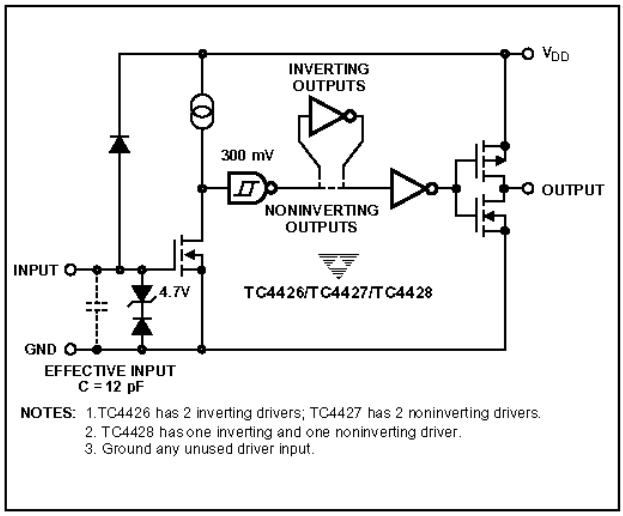
The TC4426/4427/4428 are improved versions of the earlier TC426/427/428 family of buffer/drivers (with which they are pin compatible). They will not latch up under any conditions within their power and voltage ratings. They are not subject to damage when up to 5V of noise spiking (of either polarity) occurs on the ground pin. They can accept, without damage or logic upset, up to 500mA of reverse current (of either polarity) being forced back into their outputs. All terminals are fully protected against up to 4kV of electrostatic discharge.

As MOSFET drivers, the TC4426/4427/4428 can easily switch 1000 pF gate capacitances in under 30nsec, and provide low enough impedances in both the ON and OFF states to ensure the MOSFET's intended state will not be affected, even by large transients.

Other compatible drivers are the TC4426A/27A/28A. These drivers have matched input to output leading edge and falling edge delays, tD1 and tD2, for processing short duration pulses in the 25 nanoseconds range. They are pin compatible with the TC4426/27/28.

4

FUNCTIONAL BLOCK DIAGRAM



NOTES: 1. TC4426 has 2 inverting drivers; TC4427 has 2 noninverting drivers.
2. TC4428 has one inverting and one noninverting driver.
3. Ground any unused driver input.

1.5A DUAL HIGH-SPEED POWER MOSFET DRIVERS

TC4426
TC4427
TC4428

ABSOLUTE MAXIMUM RATINGS*

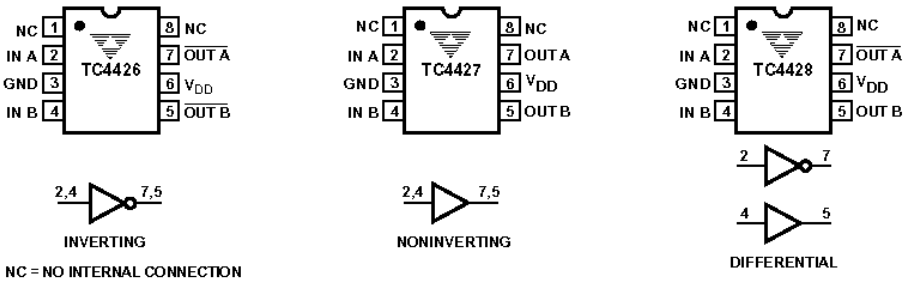
Supply Voltage ..... +22V
Input Voltage, IN A or IN B . (V_{DD} + 0.3V) to (GND – 5.0V)
Maximum Chip Temperature ..... +150°C
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Thermal Resistance
- CerDIP $R_{\theta J-A}$ ..... 150°C/W
- CerDIP $R_{\theta J-C}$ ..... 50°C/W
- PDIP $R_{\theta J-A}$ ..... 125°C/W
- PDIP $R_{\theta J-C}$ ..... 42°C/W
- SOIC $R_{\theta J-A}$ ..... 155°C/W
- SOIC $R_{\theta J-C}$ ..... 45°C/W

Operating Temperature Range
- C Version ..... 0°C to +70°C
- E Version ..... – 40°C to +85°C
- M Version ..... – 55°C to +125°C

Package Power Dissipation ($T_A \leq 70°C$)
- Plastic 730mW
- CerDIP 800mW
- SOIC 470mW

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATIONS



NC = NO INTERNAL CONNECTION
NOTE: SOIC pinout is identical to DIP.

ELECTRICAL CHARACTERISTICS: T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}	– 1	—	1	µA
Output						
V_{OH}	High Output Voltage		V_{DD} – 0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance	V_{DD} = 18V, I_O = 10 mA	—	7	10	Ω
I_{PK}	Peak Output Current	Duty Cycle ≤ 2%, t ≤ 30 µsec	—	1.5	—	A
I_{REV}	Latch-Up Protection Withstand Reverse Current	Duty Cycle ≤ 2% t ≤ 30 µsec	> 0.5	—	—	A
Switching Time (Note 1)						
t_R	Rise Time	Figure 1	—	19	30	nsec
t_F	Fall Time	Figure 1	—	19	30	nsec
t_{D1}	Delay Time	Figure 1	—	20	30	nsec
t_{D2}	Delay Time	Figure 1	—	40	50	nsec
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs) V_{IN} = 0V (Both Inputs)	— —	— —	4.5 0.4	mA mA

NOTE: 1. Switching times are guaranteed by design.

v04.0903

HMC194MS8

GaAs MMIC SPDT SWITCH DC - 3 GHz

Typical Applications

The HMC194MS8 is ideal for:

- Cellular/PCS Base Stations
- Portable Wireless
- MMDS & WirelessLAN

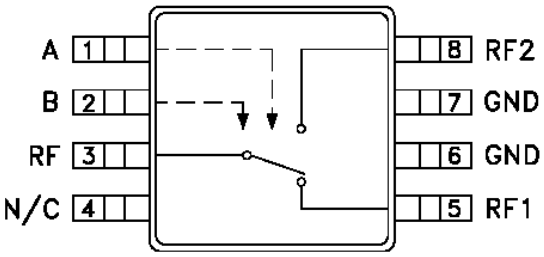
Features

Ultra Small Package: MSOP8

High Isolation: 50 dB

Positive Control: 0/+3V to 0/+7V

Functional Diagram



General Description

The HMC194MS8 is a low-cost SPDT switch in an 8-lead MSOP package for use in applications which require high isolation between two RF paths. The device can control signals from DC to 3 GHz and has been optimized to provide extremely high isolation with minimal insertion loss in medium and low power applications. On chip circuitry allows positive voltage control operation at very low DC currents with control inputs compatible with CMOS and most TTL logic families. RF1 and RF2 are reflective opens when "OFF".

Electrical Specifications, T_A = +25° C, Vctl = 0/+5 Vdc, 50 Ohm System

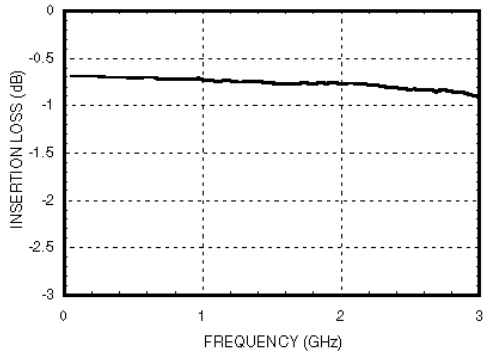
Parameter	Frequency	Min.	Typ.	Max.	Units
Insertion Loss	DC - 1.0 GHz DC - 2.0 GHz DC - 2.5 GHz DC - 3.0 GHz		0.7 0.7 0.8 0.9	0.9 0.9 1.1 1.4	dB dB dB dB
Isolation RF1 / RF2 Isolation RF1 / RF2	DC - 1.0 GHz DC - 2.0 GHz DC - 2.5 GHz DC - 3.0 GHz	45 / 47 39 / 43 31 24	49 / 51 42 / 46 35 28		dB dB dB dB
Return Loss	DC - 1.0 GHz DC - 2.0 GHz DC - 2.5 GHz DC - 3.0 GHz	18 14 13 13	21 17 17 17		dB dB dB dB
Input Power for 1 dB Compression 0/+5V Control	0.5 - 1.0 GHz 0.5 - 3.0 GHz	19 17	23 21		dBm dBm
Input Third Order Intercept 0/+5V Control (Two-tone Input Power = +7 dBm Each Tone)	0.5 - 1.0 GHz 0.5 - 3.0 GHz	39 37	43 41		dBm dBm
Switching Characteristics	DC - 3.0 GHz				
tRISE, tFALL (10/90% RF) tON , tOFF (50% CTL to 10/90% RF)			10 24		ns ns

For price, delivery, and to place orders, please contact Hittite Microwave Corporation:
12 Elizabeth Drive, Chelmsford, MA 01824 Phone: 978-250-3343 Fax: 978-250-3373
Order Online at www.hittite.com

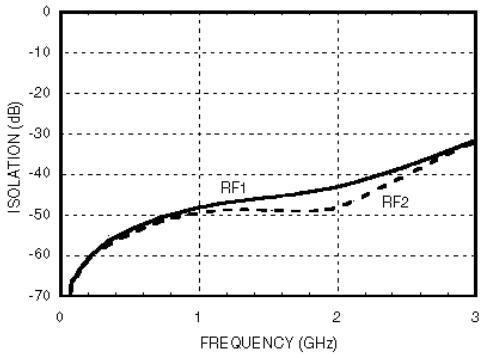
HMC194MS8

GaAs MMIC SPDT SWITCH DC - 3 GHz

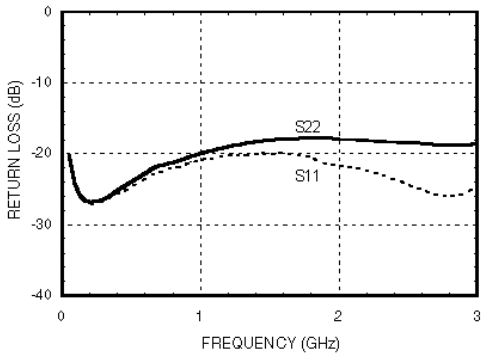
Insertion Loss



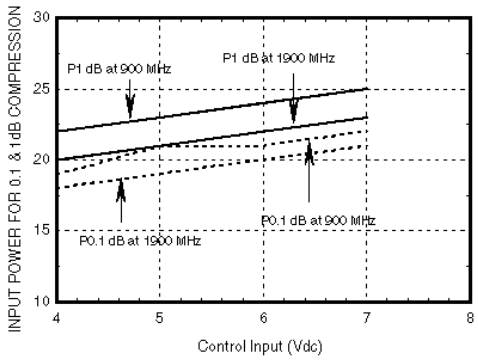
Isolation



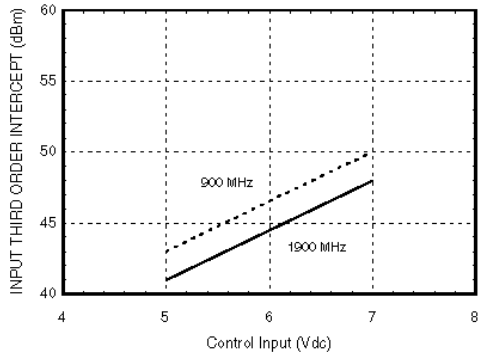
Return Loss



Input 0.1 and 1.0 dB Compression vs. Control Voltage



Input Third Order Intercept Point vs. Control Voltage



v04.0903

HMC194MS8

GaAs MMIC SPDT SWITCH DC - 3 GHz

Compression vs. Control Voltage

	Carrier at 900 MHz		Carrier at 1900 MHz	
Bias Vdd	Input Power for 0.1 dB Compression	Input Power for 1.0 dB Compression	Input Power for 0.1 dB Compression	Input Power for 1.0 dB Compression
(Vdc)	(dBm)	(dBm)	(dBm)	(dBm)
+4	19	22	18	20
+5	21	23	19	21
+6	21	24	20	22
+7	22	25	21	23

Caution: Do not operate in 1dB compression at power levels above +25 dBm and do not "hot switch" power levels greater than +18 dBm (Control = 0/+5Vdc).

DC blocks are required at ports RFC, RF1 and RF2.

Distortion vs. Control Voltage

Control Input	Third Order Intercept (dBm) +7 dBm Each Tone	
(Vdc)	900 MHz	1900 MHz
+5	43	41
+7	50	48

Truth Table

***Control Input Voltage Tolerances are ± 0.2 Vdc.**

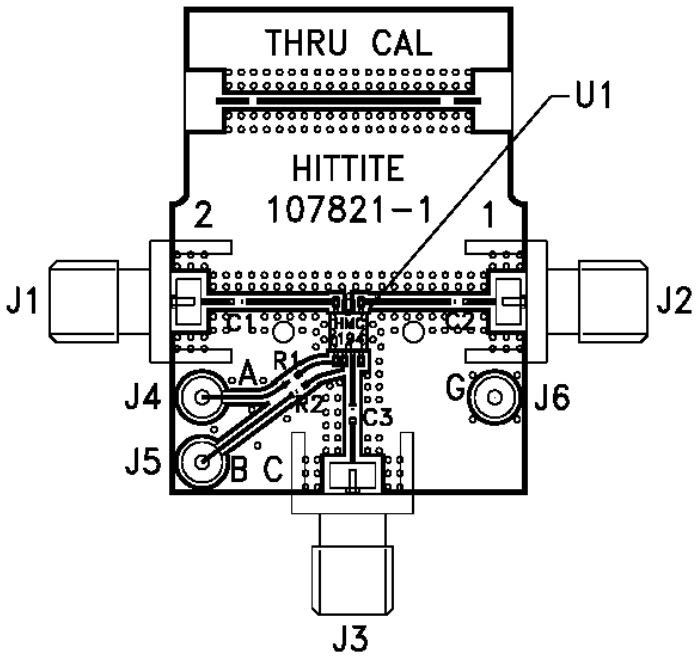
Control Input*		Control Current		Signal Path State	
A (Vdc)	B (Vdc)	Ia (uA)	Ib (uA)	RF to RF1	RF to RF2
0	+3	-23	+23	ON	OFF
+3	0	+23	-23	OFF	ON
0	+5	-95	+95	ON	OFF
+5	0	+95	-95	OFF	ON
0	+7	-190	+190	ON	OFF
+7	0	+190	-190	OFF	ON

v04.0903

HMC194MS8

GaAs MMIC SPDT SWITCH DC - 3 GHz

Evaluation Circuit Board



List of Material

Item	Description
J1 - J3	PC Mount SMA RF Connector
J4 - J6	DC Pin
C1 - C3	100 pF capacitor, 0402 Pkg.
R1, R2	100 Ω resistor, 0402 Pkg.
U1	HMC194MS8 SPDT Switch
PCB*	107821 Evaluation PCB
* Circuit Board Material: Rogers 4350	

The circuit board used in the final application should be generated with proper RF circuit design techniques. Signal lines at the RF port should have 50 ohm impedance and the package ground leads should be connected directly to the ground plane similar to that shown above. The evaluation circuit board shown above is available from Hittite Microwave Corporation upon request.

1 FEATURES

- Single power supply
- Operating supply voltage 2.5 V to 6 V
- Low standby current
- Serial input/output via I^2C-bus
- Address by 3 hardware address pins
- Sampling rate given by I^2C-bus speed
- 4 analog inputs programmable as single-ended or differential inputs
- Auto-incremented channel selection
- Analog voltage range from V_{SS} to V_{DD}
- On-chip track and hold circuit
- 8-bit successive approximation A/D conversion
- Multiplying DAC with one analog output.

2 APPLICATIONS

- Closed loop control systems
- Low power converter for remote data acquisition
- Battery operated equipment
- Acquisition of analog values in automotive, audio and TV applications.

3 GENERAL DESCRIPTION

The PCF8591 is a single-chip, single-supply low power 8-bit CMOS data acquisition device with four analog inputs, one analog output and a serial I^2C-bus interface. Three address pins A0, A1 and A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the I^2C-bus without additional hardware. Address, control and data to and from the device are transferred serially via the two-line bidirectional I^2C-bus.

The functions of the device include analog input multiplexing, on-chip track and hold function, 8-bit analog-to-digital conversion and an 8-bit digital-to-analog conversion. The maximum conversion rate is given by the maximum speed of the I^2C-bus.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8591P	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
PCF8591T	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1

5 BLOCK DIAGRAM

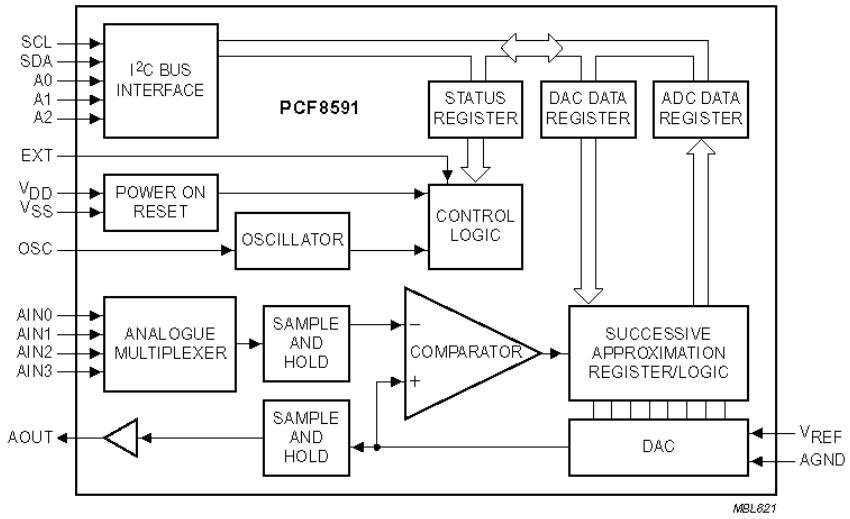


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
AINO	1	analog inputs (A/D converter)
AIN1	2	
AIN2	3	
AIN3	4	
A0	5	hardware address
A1	6	
A2	7	
V_{SS}	8	negative supply voltage
SDA	9	I^2C-bus data input/output
SCL	10	I^2C-bus clock input
OSC	11	oscillator input/output
EXT	12	external/internal switch for oscillator input
AGND	13	analog ground
V_{REF}	14	voltage reference input
AOUT	15	analog output (D/A converter)
V_{DD}	16	positive supply voltage

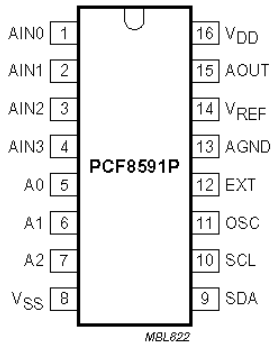


Fig.2 Pinning diagram (DIP16).

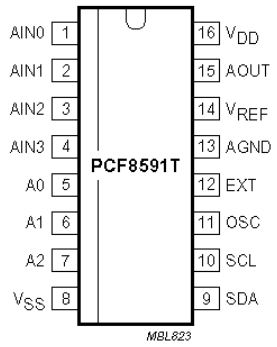


Fig.3 Pinning diagram (SO16).

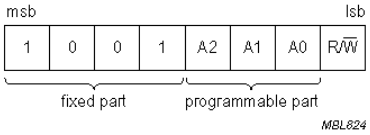


Fig.4 Address byte.

7 FUNCTIONAL DESCRIPTION

7.1 Addressing

Each PCF8591 device in an I²C-bus system is activated by sending a valid address to the device. The address consists of a fixed part and a programmable part. The programmable part must be set according to the address pins A0, A1 and A2. The address always has to be sent as the first byte after the start condition in the I²C-bus protocol. The last bit of the address byte is the read/write-bit which sets the direction of the following data transfer (see Figs 4, 16 and 17).

7.2 Control byte

The second byte sent to a PCF8591 device will be stored in its control register and is required to control the device function. The upper nibble of the control register is used for enabling the analog output, and for programming the analog inputs as single-ended or differential inputs. The lower nibble selects one of the analog input channels defined by the upper nibble (see Fig.5). If the auto-increment flag is set, the channel number is incremented automatically after each A/D conversion.

If the auto-increment mode is desired in applications where the internal oscillator is used, the analog output enable flag in the control byte (bit 6) should be set. This allows the internal oscillator to run continuously, thereby preventing conversion errors resulting from oscillator start-up delay. The analog output enable flag may be reset at other times to reduce quiescent power consumption.

The selection of a non-existing input channel results in the highest available channel number being allocated. Therefore, if the auto-increment flag is set, the next selected channel will be always channel 0. The most significant bits of both nibbles are reserved for future functions and have to be set to logic 0. After a Power-on reset condition all bits of the control register are reset to logic 0. The D/A converter and the oscillator are disabled for power saving. The analog output is switched to a high-impedance state.

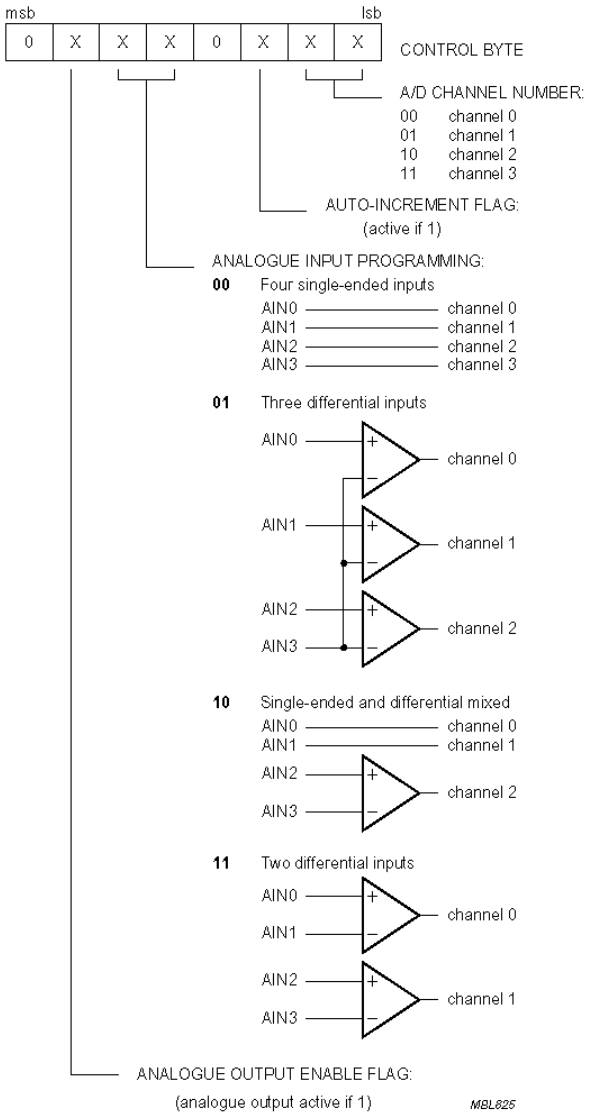


Fig.5 Control byte.

7.4 A/D conversion

The A/D converter makes use of the successive approximation conversion technique. The on-chip D/A converter and a high-gain comparator are used temporarily during an A/D conversion cycle.

An A/D conversion cycle is always started after sending a valid read mode address to a PCF8591 device. The A/D conversion cycle is triggered at the trailing edge of the acknowledge clock pulse and is executed while transmitting the result of the previous conversion (see Fig.9).

Once a conversion cycle is triggered an input voltage sample of the selected channel is stored on the chip and is converted to the corresponding 8-bit binary code. Samples picked up from differential inputs are converted to an 8-bit twos complement code (see Figs 10 and 11).

The conversion result is stored in the ADC data register and awaits transmission. If the auto-increment flag is set the next channel is selected.

The first byte transmitted in a read cycle contains the conversion result code of the previous read cycle. After a Power-on reset condition the first byte read is a hexadecimal 80. The protocol of an I^2C-bus read cycle is shown in Chapter 8, Figs 16 and 17.

The maximum A/D conversion rate is given by the actual speed of the I^2C-bus.

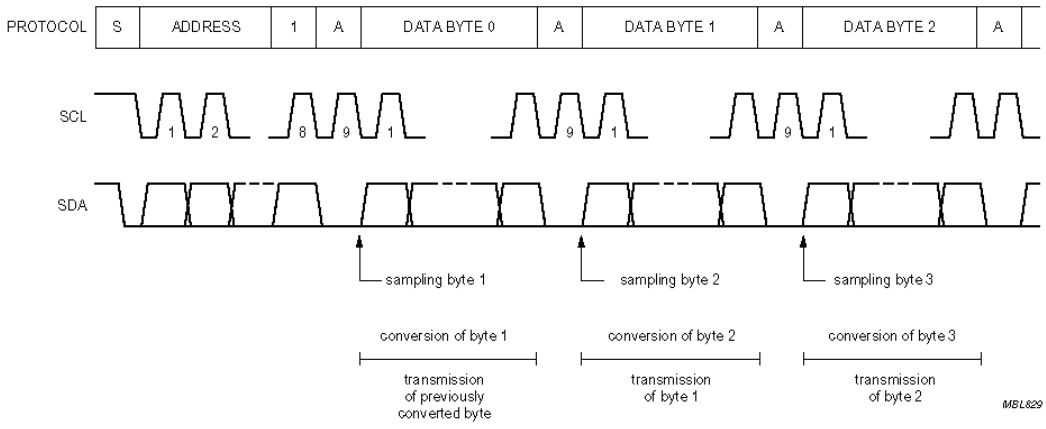


Fig.9 A/D conversion sequence.

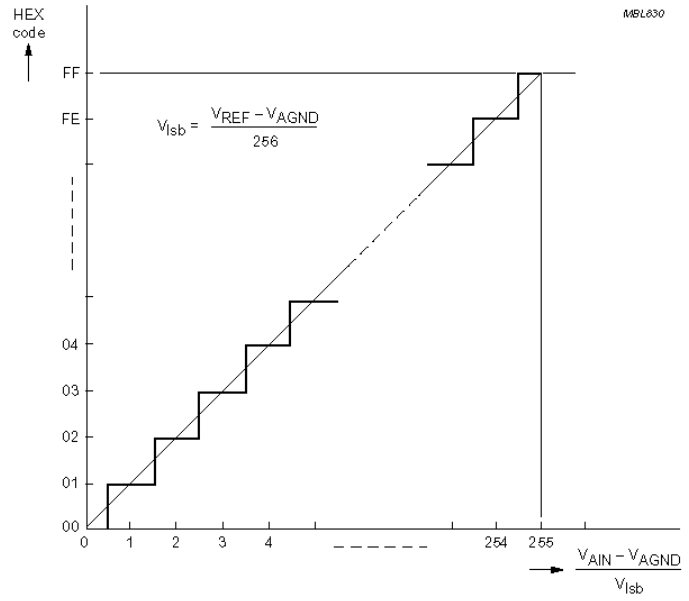


Fig.10 A/D conversion characteristics of single-ended inputs.

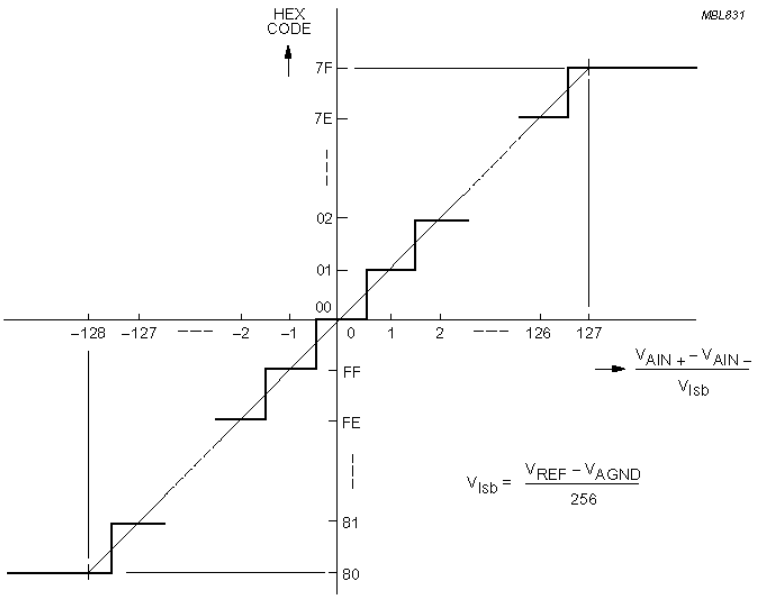


Fig.11 A/D conversion characteristics of differential inputs.

7.5 Reference voltage

For the D/A and A/D conversion either a stable external voltage reference or the supply voltage has to be applied to the resistor divider chain (pins V_{REF} and AGND). The AGND pin has to be connected to the system analog ground and may have a DC off-set with reference to V_{SS}.

A low frequency may be applied to the V_{REF} and AGND pins. This allows the use of the D/A converter as a one-quadrant multiplier; see Chapter 15 and Fig.7.

The A/D converter may also be used as a one or two quadrant analog divider. The analog input voltage is divided by the reference voltage. The result is converted to a binary code. In this application the user has to keep the reference voltage stable during the conversion cycle.

7.6 Oscillator

An on-chip oscillator generates the clock signal required for the A/D conversion cycle and for refreshing the auto-zeroed buffer amplifier. When using this oscillator the EXT pin has to be connected to V_{SS}. At the OSC pin the oscillator frequency is available.

If the EXT pin is connected to V_{DD} the oscillator output OSC is switched to a high-impedance state allowing the user to feed an external clock signal to OSC.

8 CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

8.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

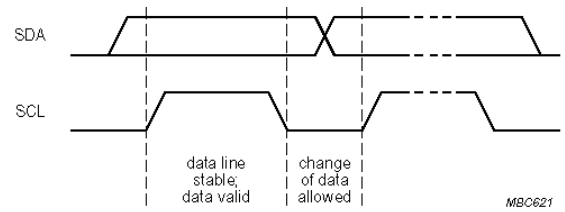


Fig.12 Bit transfer.

8.2 Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

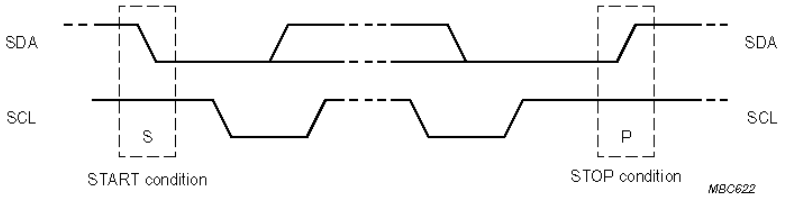


Fig.13 Definition of START and STOP condition.

8.3 System configuration

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

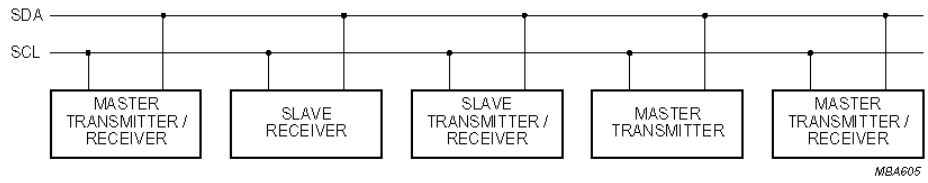


Fig.14 System configuration.

8.4 Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master also generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

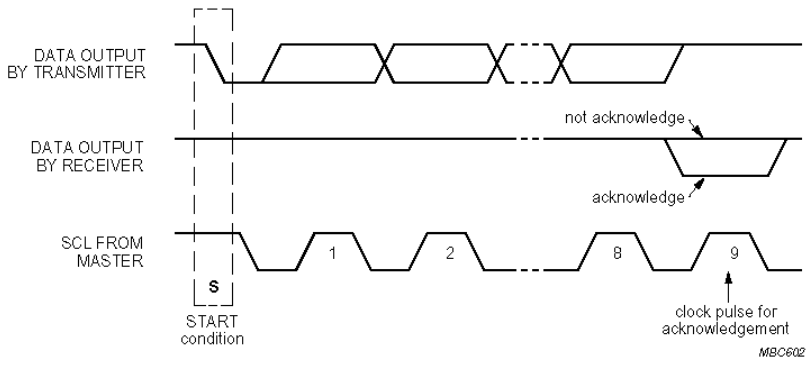


Fig.15 Acknowledgement on the I^2C-bus.

8.5 I²C-bus protocol

After a start condition a valid hardware address has to be sent to a PCF8591 device. The read/write bit defines the direction of the following single or multiple byte data transfer. For the format and the timing of the start condition (S), the stop condition (P) and the acknowledge bit (A) refer to the I²C-bus characteristics. In the write mode a data transfer is terminated by sending either a stop condition or the start condition of the next data transfer.

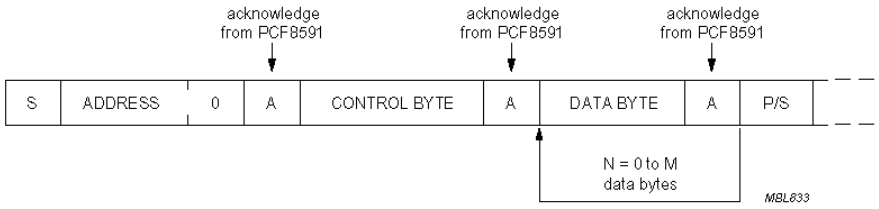


Fig.16 Bus protocol for write mode, D/A conversion.

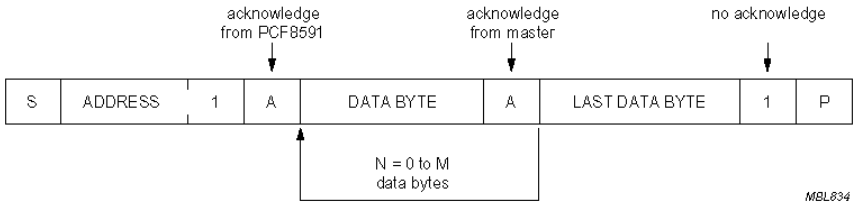


Fig.17 Bus protocol for read mode, A/D conversion.

14 AC CHARACTERISTICS

All timing values are valid within the operating supply voltage and ambient temperature range and reference to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
I²C-bus timing (see Fig.20; note 1)					
f_{SCL}	SCL clock frequency	–	–	100	kHz
t_{SP}	tolerable spike width on bus	–	–	100	ns
t_{BUF}	bus free time	4.7	–	–	µs
$t_{SU;STA}$	START condition set-up time	4.7	–	–	µs
$t_{HD;STA}$	START condition hold time	4.0	–	–	µs
t_{LOW}	SCL LOW time	4.7	–	–	µs
t_{HIGH}	SCL HIGH time	4.0	–	–	µs
t_r	SCL and SDA rise time	–	–	1.0	µs
t_f	SCL and SDA fall time	–	–	0.3	µs
$t_{SU;DAT}$	data set-up time	250	–	–	ns
$t_{HD;DAT}$	data hold time	0	–	–	ns
$t_{VD;DAT}$	SCL LOW-to-data out valid	–	–	3.4	µs
$t_{SU;STO}$	STOP condition set-up time	4.0	–	–	µs

Note

1. A detailed description of the I²C-bus specification, with applications, is given in brochure *"The I²C-bus and how to use it"*. This brochure may be ordered using the code 9398 393 40011.

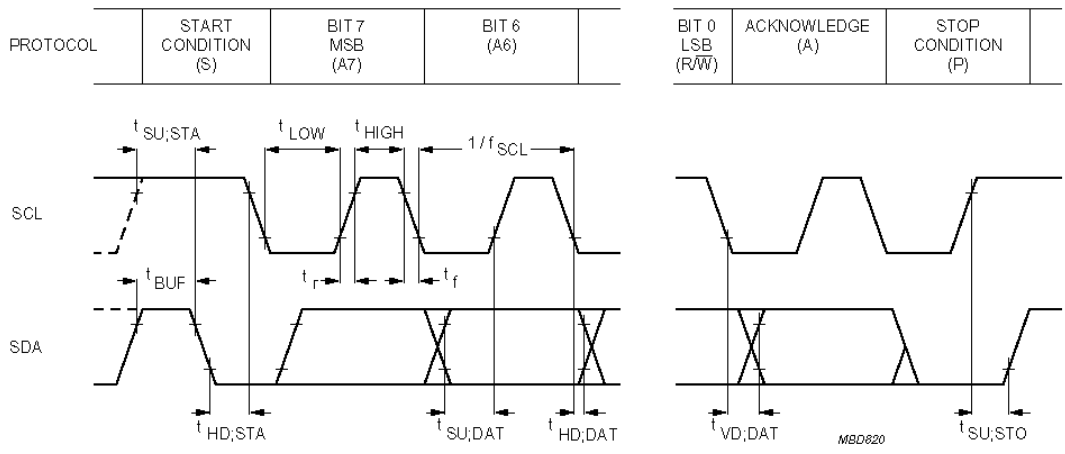


Fig.20 I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

EPCOS

Temperature Measurement **B57045**

Probe Assemblies **K 45**

Applications

- Temperature compensation (chassis mounting)
- Temperature measurement (chassis mounting)
- Temperature control (chassis mounting)

Features

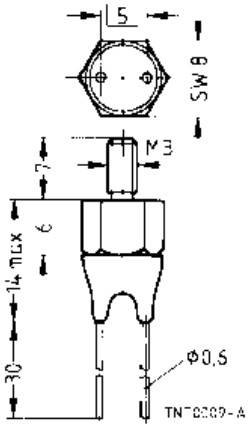
- Cost-effective
- Good thermal coupling through screw-type case (thread M3)
- Electrically isolated aluminum case
  R_{is} > 100 MΩ (V = 100 V dc); V_{is} = 2500 V (test duration: 1 s)
- Tinned copper leads

Options

Closer resistance tolerance available on request

Delivery mode

Bulk



Dimensions in mm
Approx. weight 1 g

Climatic category (IEC 60068-1)		55/125/56	
Max. power at 25 °C	P_{25}	450	mW
Resistance tolerance	$\Delta R_N/R_N$	± 10 %	
Rated temperature	T_N	25	°C
B value tolerance	$\Delta B/B$	± 3 %	
Dissipation factor (in air)	δ_{th}	approx. 9	mW/K
Dissipation factor (on chassis)	δ_{th}	approx. 20	mW/K
Thermal cooling time constant (in air)	τ_c	approx. 75	s
Thermal cooling time constant (on chassis)	τ_c	approx. 15	s
Torque		approx. 0,5	Nm

R_{25} Ω	No. of R/T characteristic	$B_{25/100}$ K	Ordering code
1 k	1011	3730	B57045K0102K000
2,2 k	1013	3900	B57045K0222K000
4,7 k	4001	3950	B57045K0472K000
6,8 k	2903	4200	B57045K0682K000
10,0 k	2904	4300	B57045K0103K000
33 k	1012	4300	B57045K0333K000
47 k	4003	4450	B57045K0473K000
68 k	2005	4600	B57045K0683K000
100 k	2005	4600	B57045K0104K000
150 k	2005	4600	B57045K0154K000

EPCOS

Standardized *R/T* Characteristics

1 Introduction

1.1 Resistance value

The *R/T* characteristics tabulated in the following have been standardized for the resistance value at 25 °C. The actual resistance values of a particular NTC thermistor are obtained by multiplying the ratio R_T/R_{25} (tabulated value) by the resistance value at 25 °C (specified in the data sheets).

$$R_T = \frac{R_T}{R_{25}} \cdot R_{25} \qquad (1)$$

Resistance values at intermediate temperatures within the range of the subsequent temperature interval can be calculated by means of the temperature coefficient α.

α is inserted in the following equation:

$$R_T = R_{T_x} \cdot \exp\left[\frac{\alpha_x}{100} \cdot (T_x + 273{,}15)^2 \cdot \left(\frac{1}{T + 273{,}15} - \frac{1}{T_x + 273{,}15}\right)\right] \qquad (2)$$

R_T Resistance value at temperature T
R_{Tx} Resistance value at the beginning of the relevant temperature interval
T_x Temperature in °C at the beginning of the relevant temperature interval
T Temperature of interest in °C ($T_x < T < T_{x+1}$)
α_x Temperature coefficient at temperature T_x

Example:

Given: Curve 1006
R_{25} = 4,7 kΩ
α_5 = 4,4
Unknown: Resistance at 7 °C (R_7)

a) Calculation of the resistance value at the beginning of the relevant temperature interval (T_x = 5 °C):

$$R_{T_x} = R_5 = 2{,}2739 \cdot 4{,}7\ \text{k}\Omega = 10{,}6873\ \text{k}\Omega$$

b) Substituting this value into equation (2) yields:

$$R_7 = R_5 \cdot \exp\left[\frac{\alpha_5}{100} \cdot (5 + 273{,}15)^2 \cdot \left(\frac{1}{7 + 273{,}15} - \frac{1}{5 + 273{,}15}\right)\right]$$

$$R_7 = 10{,}6873\ \text{k}\Omega \cdot \exp\left[\frac{4{,}4}{100} \cdot 278{,}15^2 \cdot \left(\frac{1}{280{,}15} - \frac{1}{278{,}15}\right)\right]$$

$$R_7 = 10{,}6873\ \text{k}\Omega \cdot \exp[-0{,}08737] = 10{,}6873 \cdot 0{,}9163$$

$$R_7 = 9{,}7932\ \text{k}\Omega$$

EPCOS

Standardized *R/T* Characteristics

Number	2014		2101		2901		2903	
T (°C)	$B_{25/100}$ = 4540 K		$B_{25/100}$ = 4100 K		$B_{25/100}$ = 3760 K		$B_{25/100}$ = 4200 K	
	R_T/R_{25}	α (%/K)	R_T/R_{25}	α (%/K)	R_T/R_{25}	α (%/K)	R_T/R_{25}	α (%/K)
– 55,0	142,00	7,8	104,09	7,5	63,969	6,7	120,03	7,7
– 50,0	96,615	7,6	72,101	7,2	46,179	6,4	82,380	7,4
– 45,0	66,562	7,3	50,572	7,0	33,738	6,2	57,248	7,2
– 40,0	46,400	7,1	35,898	6,7	24,927	6,0	40,255	7,0
– 35,0	32,708	6,9	25,774	6,5	18,611	5,8	28,627	6,7
– 30,0	23,302	6,7	18,707	6,3	14,033	5,6	20,577	6,6
– 25,0	16,770	6,5	13,720	6,1	10,679	5,4	14,876	6,4
– 20,0	12,186	6,3	10,163	5,9	8,1980	5,3	10,880	6,1
– 15,0	8,9370	6,1	7,5998	5,7	6,3123	5,2	8,0808	5,9
– 10,0	6,6125	5,9	5,7351	5,5	4,9014	5,1	6,0612	5,8
– 5,0	4,9342	5,8	4,3657	5,4	3,8210	4,9	4,5649	5,6
0,0	3,7120	5,6	3,3511	5,2	3,0027	4,7	3,4708	5,4
5,0	2,8145	5,5	2,5929	5,1	2,3801	4,6	2,6625	5,2
10,0	2,1500	5,3	2,0216	4,9	1,9000	4,5	2,0599	5,1
15,0	1,6544	5,2	1,5878	4,8	1,5257	4,3	1,6069	4,9
20,0	1,2819	5,0	1,2558	4,6	1,2330	4,3	1,2631	4,8
25,0	1,0000	4,9	1,0000	4,5	1,0000	4,1	1,0000	4,6
30,0	0,78514	4,8	0,80145	4,4	0,81679	4,0	0,79593	4,5
35,0	0,62031	4,7	0,64632	4,2	0,67166	3,9	0,63796	4,4
40,0	0,49304	4,5	0,52433	4,1	0,55527	3,8	0,51467	4,2
45,0	0,39417	4,4	0,42781	4,0	0,46095	3,8	0,41887	4,1
50,0	0,31690	4,3	0,35099	3,9	0,38459	3,7	0,34272	4,0
55,0	0,25616	4,2	0,28949	3,8	0,32184	3,6	0,28081	3,9
60,0	0,20815	4,1	0,23998	3,7	0,27068	3,5	0,23141	3,8
65,0	0,17000	4,0	0,19992	3,6	0,22907	3,3	0,19211	3,7
70,0	0,13952	3,9	0,16733	3,5	0,19468	3,2	0,16027	3,6
75,0	0,11505	3,8	0,14070	3,4	0,16607	3,1	0,13421	3,5
80,0	0,095302	3,7	0,11882	3,3	0,14221	3,1	0,11288	3,4
85,0	0,079296	3,6	0,10077	3,3	0,12218	3,0	0,095326	3,3
90,0	0,066263	3,5	0,085806	3,2	0,10533	2,9	0,080828	3,2
95,0	0,055601	3,5	0,073354	3,1	0,09123	2,8	0,068916	3,2
100,0	0,046843	3,4	0,062947	3,0	0,079284	2,8	0,058989	3,1
105,0	0,039618	3,3	0,054214	3,0	0,069062	2,7	0,050701	3,0
110,0	0,033634	3,2	0,046858	2,9	0,060340	2,7	0,043735	3,0
115,0	0,028658	3,2	0,040638	2,8	0,052886	2,6	0,037778	2,9
120,0	0,024505	3,1	0,035361	2,8	0,046482	2,5	0,032736	2,8
125,0	0,021026	3,0	0,030866	2,7	0,040985	2,5	0,028513	2,7
130,0	0,018101	3,0	–	–	0,036233	2,5	–	–
135,0	0,015633	2,9	–	–	0,032101	2,4	–	–

Complete 10-Bit, 20 MSPS, 80 mW CMOS A/D Converter

AD9200

FEATURES
CMOS 10-Bit, 20 MSPS Sampling A/D Converter
Pin-Compatible with AD876
Power Dissipation: 80 mW (3 V Supply)
Operation Between 2.7 V and 5.5 V Supply
Differential Nonlinearity: 0.5 LSB
Power-Down (Sleep) Mode
Three-State Outputs
Out-of-Range Indicator
Built-In Clamp Function (DC Restore)
Adjustable On-Chip Voltage Reference
IF Undersampling to 135 MHz

PRODUCT DESCRIPTION

The AD9200 is a monolithic, single supply, 10-bit, 20 MSPS analog-to-digital converter with an on-chip sample-and-hold amplifier and voltage reference. The AD9200 uses a multistage differential pipeline architecture at 20 MSPS data rates and guarantees no missing codes over the full operating temperature range.

The input of the AD9200 has been designed to ease the development of both imaging and communications systems. The user can select a variety of input ranges and offsets and can drive the input either single-ended or differentially.

The sample-and-hold (SHA) amplifier is equally suited for both multiplexed systems that switch full-scale voltage levels in successive channels and sampling single-channel inputs at frequencies up to and beyond the Nyquist rate. AC coupled input signals can be shifted to a predetermined level, with an onboard clamp circuit (AD9200ARS, AD9200KST). The dynamic performance is excellent.

The AD9200 has an onboard programmable reference. An external reference can also be chosen to suit the dc accuracy and temperature drift requirements of the application.

A single clock input is used to control all internal conversion cycles. The digital output data is presented in straight binary output format. An out-of-range signal (OTR) indicates an overflow condition which can be used with the most significant bit to determine low or high overflow.

The AD9200 can operate with supply range from 2.7 V to 5.5 V, ideally suiting it for low power operation in high speed portable applications.

The AD9200 is specified over the industrial (–40°C to +85°C) and commercial (0°C to +70°C) temperature ranges.

PRODUCT HIGHLIGHTS

Low Power
The AD9200 consumes 80 mW on a 3 V supply (excluding the reference power). In sleep mode, power is reduced to below 5 mW.

Very Small Package
The AD9200 is available in both a 28-lead SSOP and 48-lead LQFP packages.

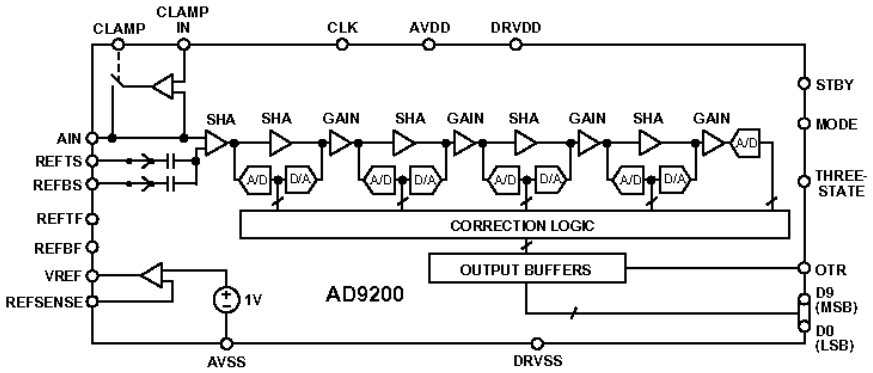
Pin Compatible with AD876
The AD9200 is pin compatible with the AD876, allowing older designs to migrate to lower supply voltages.

300 MHz On-Board Sample-and-Hold
The versatile SHA input can be configured for either single-ended or differential inputs.

Out-of-Range Indicator
The OTR output bit indicates when the input signal is beyond the AD9200's input range.

Built-In Clamp Function
Allows dc restoration of video signals with AD9200ARS and AD9200KST.

FUNCTIONAL BLOCK DIAGRAM



REV. E

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

AD9200–SPECIFICATIONS

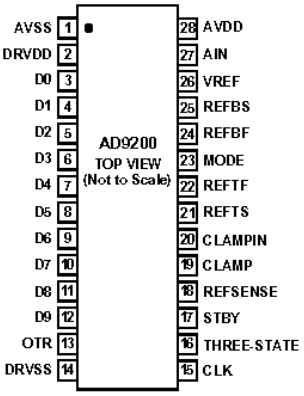
(AVDD = +3 V, DRVDD = +3 V, F_S = 20 MHz (50% Duty Cycle), MODE = AVDD, 2 V Input Span from 0.5 V to 2.5 V, External Reference, T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Units	Condition
RESOLUTION			10		Bits	
CONVERSION RATE	F_S			20	MHz	
DC ACCURACY						
Differential Nonlinearity	DNL		±0.5	±1	LSB	REFTS = 2.5 V, REFBS = 0.5 V
Integral Nonlinearity	INL		±0.75	±2	LSB	
Offset Error	E_{ZS}		0.4	1.2	% FSR	
Gain Error	E_{FS}		1.4	3.5	% FSR	
REFERENCE VOLTAGES						
Top Reference Voltage	REFTS	1		AVDD	V	
Bottom Reference Voltage	REFBS	GND		AVDD – 1	V	
Differential Reference Voltage			2		V p-p	
Reference Input Resistance[1]			10		kΩ	REFTS, REFBS: MODE = AVDD
			4.2		kΩ	Between REFTF and REFBF: MODE = AVSS
ANALOG INPUT						
Input Voltage Range	AIN	REFBS		REFTS	V	REFBS Min = GND: REFTS Max = AVDD
Input Capacitance	C_{IN}		1		pF	Switched
Aperture Delay	t_{AP}		4		ns	
Aperture Uncertainty (Jitter)	t_{AJ}		2		ps	
Input Bandwidth (–3 dB)	BW					
Full Power (0 dB)			300		MHz	
DC Leakage Current			23		µA	Input = ±FS
INTERNAL REFERENCE						
Output Voltage (1 V Mode)	VREF		1		V	REFSENSE = VREF
Output Voltage Tolerance (1 V Mode)			±10	±25	mV	
Output Voltage (2 V Mode)	VREF		2		V	REFSENSE = GND
Load Regulation (1 V Mode)			0.5	2	mV	1 mA Load Current
POWER SUPPLY						
Operating Voltage	AVDD	2.7	3	5.5	V	
	DRVDD	2.7	3	5.5	V	
Supply Current	IAVDD		26.6	33.3	mA	AVDD = 3 V, MODE = AVSS
Power Consumption	P_D		80	100	mW	AVDD = DRVDD = 3 V, MODE = AVSS
Power-Down			4		mW	STBY = AVDD, MODE and CLOCK = AVSS
Gain Error Power Supply Rejection	PSRR		1		% FS	
DYNAMIC PERFORMANCE (AIN = 0.5 dBFS)						
Signal-to-Noise and Distortion	SINAD					
f = 3.58 MHz		54.5	57		dB	
f = 10 MHz			54		dB	
Effective Bits						
f = 3.58 MHz			9.1		Bits	
f = 10 MHz			8.6		Bits	
Signal-to-Noise	SNR					
f = 3.58 MHz		55	57		dB	
f = 10 MHz			56		dB	
Total Harmonic Distortion	THD					
f = 3.58 MHz		–59	–66		dB	
f = 10 MHz			–58		dB	
Spurious Free Dynamic Range	SFDR					
f = 3.58 MHz		–61	–69		dB	
f = 10 MHz			–61		dB	
Two-Tone Intermodulation Distortion	IMD		68		dB	f = 44.49 MHz and 45.52 MHz
Differential Phase	DP		0.1		Degree	NTSC 40 IRE Mod Ramp
Differential Gain	DG		0.05		%	

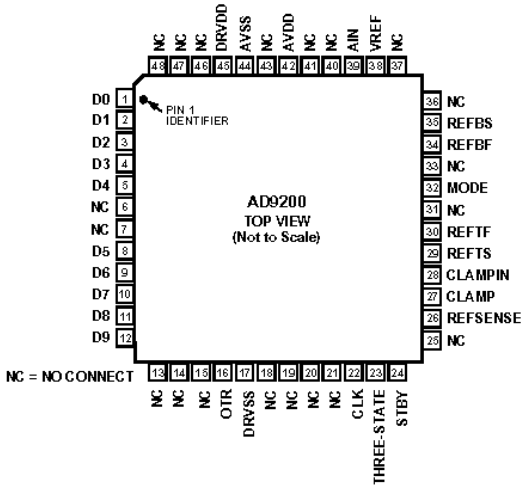
AD9200

PIN CONFIGURATIONS

28-Lead Shrink Small Outline (SSOP)



48-Lead Plastic Thin Quad Flatpack (LQFP)



PIN FUNCTION DESCRIPTIONS

SSOP Pin No.	LQFP Pin No.	Name	Description
1	44	AVSS	Analog Ground
2	45	DRVDD	Digital Driver Supply
3	1	D0	Bit 0, Least Significant Bit
4	2	D1	Bit 1
5	3	D2	Bit 2
6	4	D3	Bit 3
7	5	D4	Bit 4
8	8	D5	Bit 5
9	9	D6	Bit 6
10	10	D7	Bit 7
11	11	D8	Bit 8
12	12	D9	Bit 9, Most Significant Bit
13	16	OTR	Out-of-Range Indicator
14	17	DRVSS	Digital Ground
15	22	CLK	Clock Input
16	23	THREE-STATE	HI: High Impedance State. LO: Normal Operation
17	24	STBY	HI: Power-Down Mode. LO: Normal Operation
18	26	REFSENSE	Reference Select
19	27	CLAMP	HI: Enable Clamp Mode. LO: No Clamp
20	28	CLAMPIN	Clamp Reference Input
21	29	REFTS	Top Reference
22	30	REFTF	Top Reference Decoupling
23	32	MODE	Mode Select
24	34	REFBF	Bottom Reference Decoupling
25	35	REFBS	Bottom Reference
26	38	VREF	Internal Reference Output
27	39	AIN	Analog Input
28	42	AVDD	Analog Supply

AD9200

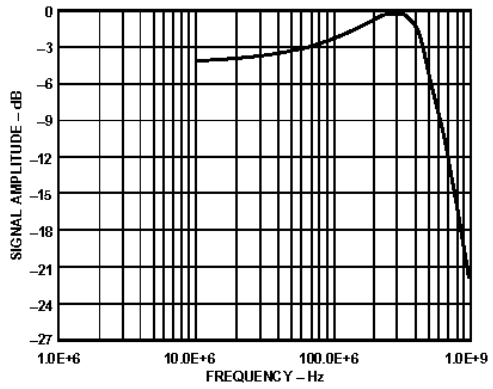


Figure 13. Full Power Bandwidth

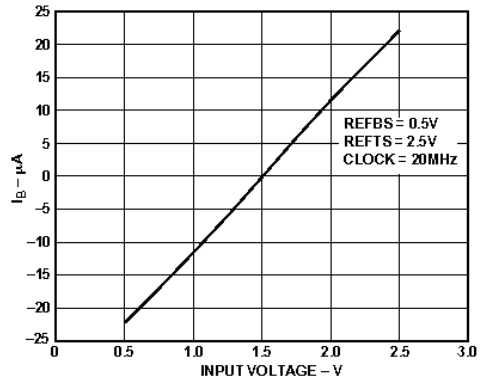


Figure 14. Input Bias Current vs. Input Voltage

APPLYING THE AD9200

THEORY OF OPERATION

The AD9200 implements a pipelined multistage architecture to achieve high sample rate with low power. The AD9200 distributes the conversion over several smaller A/D subblocks, refining the conversion with progressively higher accuracy as it passes the results from stage to stage. As a consequence of the distributed conversion, the AD9200 requires a small fraction of the 1023 comparators used in a traditional flash type A/D. A sample-and-hold function within each of the stages permits the first stage to operate on a new input sample while the second, third and fourth stages operate on the three preceding samples.

OPERATIONAL MODES

The AD9200 is designed to allow optimal performance in a wide variety of imaging, communications and instrumentation applications, including pin compatibility with the AD876 A/D. To realize this flexibility, internal switches on the AD9200 are used to reconfigure the circuit into different modes. These modes are selected by appropriate pin strapping. There are three parts of the circuit affected by this modality: the voltage reference, the reference buffer, and the analog input. The nature of the application will determine which mode is appropriate: the descriptions in the following sections, as well as the Table I should assist in picking the desired mode.

Table I. Mode Selection

Modes	Input Connect	Input Span	MODE Pin	REFSENSE Pin	REF	REFTS	REFBS	Figure
TOP/BOTTOM	AIN	1 V	AVDD	Short REFSENSE, REFTS and VREF Together			AGND	18
	AIN	2 V	AVDD	AGND	Short REFTS and VREF Together		AGND	19
CENTER SPAN	AIN	1 V	AVDD/2	Short VREF and REFSENSE Together		AVDD/2	AVDD/2	20
	AIN	2 V	AVDD/2	AGND	No Connect	AVDD/2	AVDD/2	
Differential	AIN Is Input 1	1 V	AVDD/2	Short VREF and REFSENSE Together		AVDD/2	AVDD/2	29
	REFTS and REFBS Are Shorted Together for Input 2	2 V	AVDD/2	AGND	No Connect	AVDD/2	AVDD/2	
External Ref	AIN	2 V max	AVDD	AVDD	No Connect	Span = REFTS – REFBS (2 V max)		21, 22
			AGND			Short to VREFTF	Short to VREFBF	23
AD876	AIN	2 V	Float or AVSS	AVDD	No Connect	Short to VREFTF	Short to VREFBF	30

AD9200

SUMMARY OF MODES

VOLTAGE REFERENCE

1 V Mode the internal reference may be set to 1 V by connecting REFSENSE and VREF together.

2 V Mode the internal reference my be set to 2 V by connecting REFSENSE to analog ground

External Divider Mode the internal reference may be set to a point between 1 V and 2 V by adding external resistors. See Figure 16f.

External Reference Mode enables the user to apply an external reference to REFTS, REFBS and VREF pins. This mode is attained by tying REFSENSE to VDD.

REFERENCE BUFFER

Center Span Mode midscale is set by shorting REFTS and REFBS together and applying the midscale voltage to that point The MODE pin is set to AVDD/2. The analog input will swing about that midscale point.

Top/Bottom Mode sets the input range between two points. The two points are between 1 V and 2 V apart. The Top/Bottom Mode is enabled by tying the MODE pin to AVDD.

ANALOG INPUT

Differential Mode is attained by driving the AIN pin as one differential input and shorting REFTS and REFBS together and driving them as the second differential input. The MODE pin is tied to AVDD/2. Preferred mode for optimal distortion performance.

Single-Ended is attained by driving the AIN pin while the REFTS and REFBS pins are held at dc points. The MODE pin is tied to AVDD.

Single-Ended/Clamped (AC Coupled) the input may be clamped to some dc level by ac coupling the input. This is done by tying the CLAMPIN to some dc point and applying a pulse to the CLAMP pin. MODE pin is tied to AVDD.

SPECIAL

AD876 Mode enables users of the AD876 to drop the AD9200 into their socket. This mode is attained by floating or grounding the MODE pin.

INPUT AND REFERENCE OVERVIEW

Figure 16, a simplified model of the AD9200, highlights the relationship between the analog input, AIN, and the reference voltages, REFTS, REFBS and VREF. Like the voltages applied to the resistor ladder in a flash A/D converter, REFTS and REFBS define the maximum and minimum input voltages to the A/D.

The input stage is normally configured for single-ended operation, but allows for differential operation by shorting REFTS and REFBS together to be used as the second input.

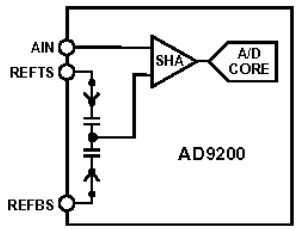


Figure 15. AD9200 Equivalent Functional Input Circuit

In single-ended operation, the input spans the range,

$$REFBS \leq AIN \leq REFTS$$

where *REFBS* can be connected to GND and REFTS connected to VREF. If the user requires a different reference range, REFBS and REFTS can be driven to any voltage within the power supply rails, so long as the difference between the two is between 1 V and 2 V.

In differential operation, REFTS and REFBS are shorted together, and the input span is set by VREF,

$$(REFTS - VREF/2) \leq AIN \leq (REFTS + VREF/2)$$

where *VREF* is determined by the internal reference or brought in externally by the user.

The best noise performance may be obtained by operating the AD9200 with a 2 V input range. The best distortion performance may be obtained by operating the AD9200 with a 1 V input range.

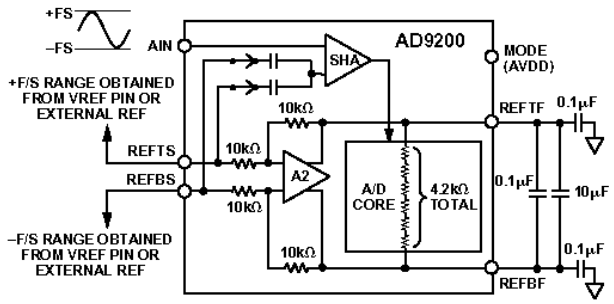
REFERENCE OPERATION

The AD9200 can be configured in a variety of reference topologies. The simplest configuration is to use the AD9200's onboard bandgap reference, which provides a pin-strappable option to generate either a 1 V or 2 V output. If the user desires a reference voltage other than those two, an external resistor divider can be connected between VREF, REFSENSE and analog ground to generate a potential anywhere between 1 V and 2 V. Another alternative is to use an external reference for designs requiring enhanced accuracy and/or drift performance. A third alternative is to bring in top and bottom references, bypassing VREF altogether.

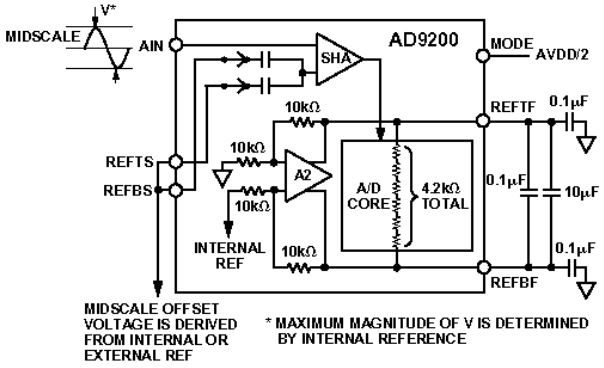
Figures 16d, 16e and 16f illustrate the reference and input architecture of the AD9200. In tailoring a desired arrangement, the user can select an input configuration to match drive circuit. Then, moving to the reference modes at the bottom of the figure, select a reference circuit to accommodate the offset and amplitude of a full-scale signal.

Table I outlines pin configurations to match user requirements.

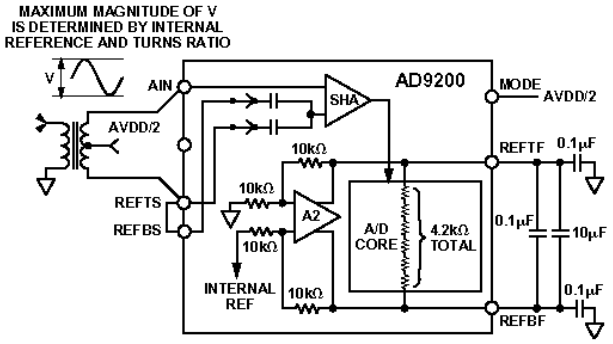
AD9200



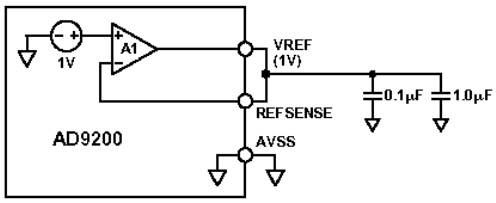
a. Top/Bottom Mode



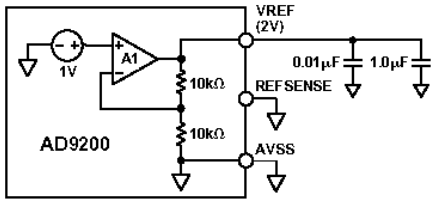
b. Center Span Mode



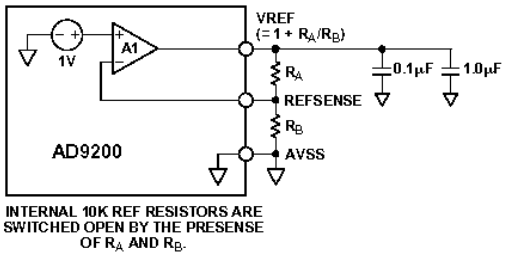
c. Differential Mode



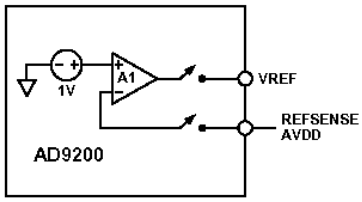
d. 1 V Reference



e. 2 V Reference



f. Variable Reference
(Between 1 V and 2 V)



g. Internal Reference Disable
(Power Reduction)

Figure 16.

AD9200

The actual reference voltages used by the internal circuitry of the AD9200 appear on REFTF and REFBF. For proper operation, it is necessary to add a capacitor network to decouple these pins. The REFTF and REFBF should be decoupled for all internal and external configurations as shown in Figure 17.

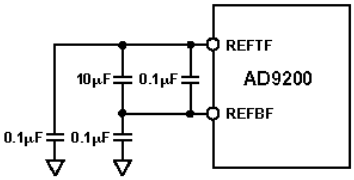


Figure 17. Reference Decoupling Network

Note: REFTF = reference top, force
REFBF = reference bottom, force
REFTS = reference top, sense
REFBS = reference bottom, sense

INTERNAL REFERENCE OPERATION

Figures 18, 19 and 20 show example hookups of the AD9200 internal reference in its most common configurations. (Figures 18 and 19 illustrate top/bottom mode while Figure 20 illustrates center span mode). Figure 29 shows how to connect the AD9200 for 1 V p-p differential operation. Shorting the VREF pin directly to the REFSENSE pin places the internal reference amplifier, A1, in unity-gain mode and the resultant reference output is 1 V. In Figure 18 REFBS is grounded to give an input range from 0 V to 1 V. These modes can be chosen when the supply is either +3 V or +5 V. The VREF pin must be bypassed to AVSS (analog ground) with a 1.0 µF tantalum capacitor in parallel with a low inductance, low ESR, 0.1 µF ceramic capacitor.

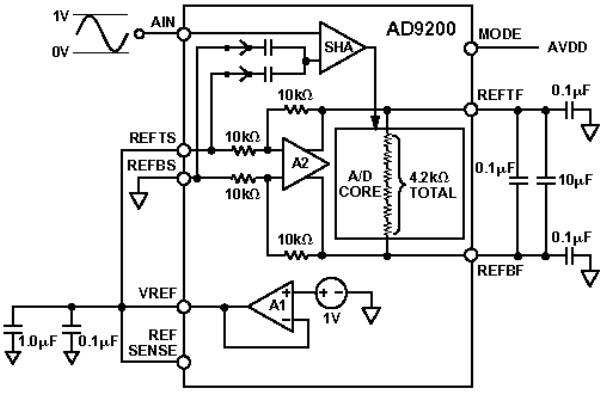


Figure 18. Internal Reference 1 V p-p Input Span (Top/Bottom Mode)

Figure 19 shows the single-ended configuration for 2 V p-p operation. REFSENSE is connected to GND, resulting in a 2 V reference output.

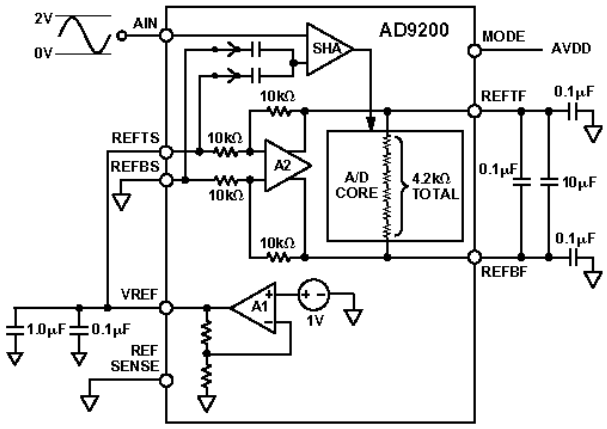


Figure 19. Internal Reference, 2 V p-p Input Span (Top/Bottom Mode)

Figure 20 shows the single-ended configuration that gives the good high frequency dynamic performance (SINAD, SFDR). To optimize dynamic performance, center the common-mode voltage of the analog input at approximately 1.5 V. Connect the shorted REFTS and REFBS inputs to a low impedance 1.5 V source. In this configuration, the MODE pin is driven to a voltage at midsupply (AVDD/2).

Maximum reference drive is 1 mA. An external buffer is required for heavier loads.

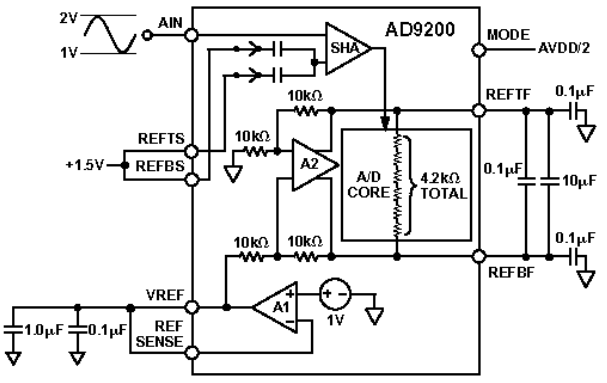


Figure 20. Internal Reference 1 V p-p Input Span, (Center Span Mode)

AD9200

DIFFERENTIAL INPUT OPERATION

The AD9200 will accept differential input signals. This function may be used by shorting REFTS and REFBS and driving them as one leg of the differential signal (the top leg is driven into AIN). In the configuration below, the AD9200 is accepting a 1 V p-p signal. See Figure 29.

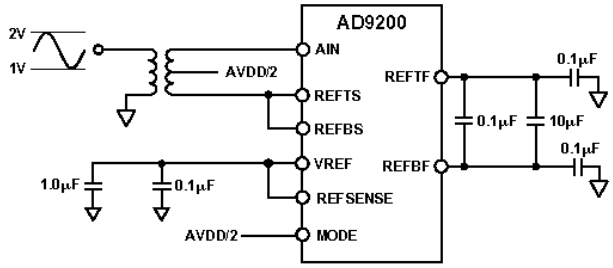


Figure 29. Differential Input

AD876 MODE OF OPERATION

The AD9200 may be dropped into the AD876 socket. This will allow AD876 users to take advantage of the reduced power consumption realized when running the AD9200 on a 3.0 V analog supply.

Figure 30 shows the pin functions of the AD876 and AD9200. The grounded REFSENSE pin and floating MODE pin effectively put the AD9200 in the external reference mode. The external reference input for the AD876 will now be placed on the reference pins of the AD9200.

The clamp controls will be grounded by the AD876 socket. The AD9200 has a 3 clock cycle delay compared to a 3.5 cycle delay of the AD876.

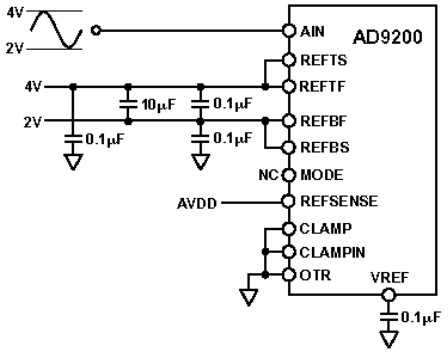


Figure 30. AD876 Mode

CLOCK INPUT

The AD9200 clock input is buffered internally with an inverter powered from the AVDD pin. This feature allows the AD9200 to accommodate either +5 V or +3.3 V CMOS logic input signal swings with the input threshold for the CLK pin nominally at AVDD/2.

The pipelined architecture of the AD9200 operates on both rising and falling edges of the input clock. To minimize duty cycle variations the recommended logic family to drive the clock input is high speed or advanced CMOS (HC/HCT, AC/ACT) logic. CMOS logic provides both symmetrical voltage threshold levels and sufficient rise and fall times to support 20 MSPS operation. The AD9200 is designed to support a conversion rate of 20 MSPS; running the part at slightly faster clock rates may be possible, although at reduced performance levels. Conversely, some slight performance improvements might be realized by clocking the AD9200 at slower clock rates.

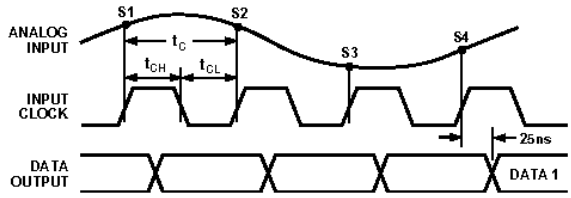


Figure 31. Timing Diagram

The power dissipated by the output buffers is largely proportional to the clock frequency; running at reduced clock rates provides a reduction in power consumption.

DIGITAL INPUTS AND OUTPUTS

Each of the AD9200 digital control inputs, THREE-STATE and STBY are reference to analog ground. The clock is also referenced to analog ground.

The format of the digital output is straight binary (see Figure 32). A low power mode feature is provided such that for STBY = HIGH and the clock disabled, the static power of the AD9200 will drop below 5 mW.

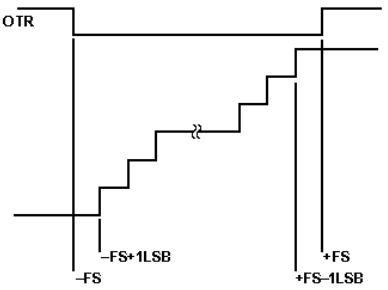


Figure 32. Output Data Format

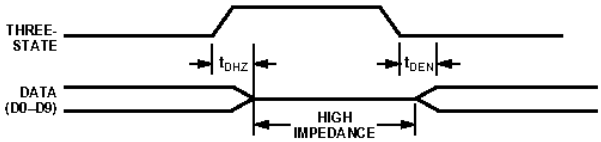


Figure 33. Three-State Timing Diagram

LINEAR TECHNOLOGY

LT1358/LT1359

Dual and Quad 25MHz, 600V/µs Op Amps

FEATURES

- **25MHz Gain Bandwidth**
- **600V/µs Slew Rate**
- **2.5mA Maximum Supply Current per Amplifier**
- Unity-Gain Stable
- C-Load™ Op Amp Drives All Capacitive Loads
- 8nV/√Hz Input Noise Voltage
- 600µV Maximum Input Offset Voltage
- 500nA Maximum Input Bias Current
- 120nA Maximum Input Offset Current
- 20V/mV Minimum DC Gain, R_L=1k
- 115ns Settling Time to 0.1%, 10V Step
- 220ns Settling Time to 0.01%, 10V Step
- ±12.5V Minimum Output Swing into 500Ω
- ±3V Minimum Output Swing into 150Ω
- Specified at ±2.5V, ±5V, and ±15V

APPLICATIONS

- Wideband Amplifiers
- Buffers
- Active Filters
- Data Acquisition Systems
- Photodiode Amplifiers

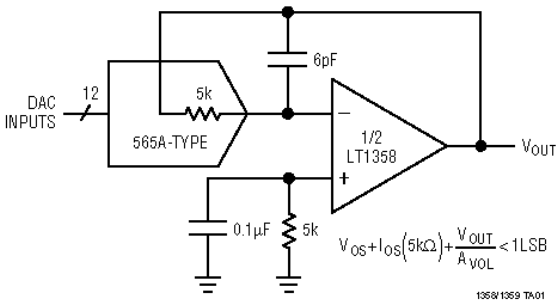
DESCRIPTION

The LT1358/LT1359 are dual and quad low power high speed operational amplifiers with outstanding AC and DC performance. The amplifiers feature much lower supply current and higher slew rate than devices with comparable bandwidth. The circuit topology is a voltage feedback amplifier with matched high impedance inputs and the slewing performance of a current feedback amplifier. The high slew rate and single stage design provide excellent settling characteristics which make the circuit an ideal choice for data acquisition systems. Each output drives a 500Ω load to ±12.5V with ±15V supplies and a 150Ω load to ±3V on ±5V supplies. The amplifiers are stable with any capacitive load making them useful in buffer applications.

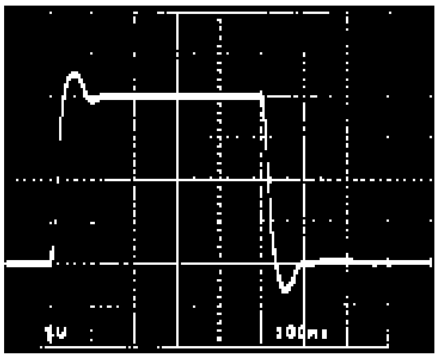
The LT1358/LT1359 are members of a family of fast, high performance amplifiers using this unique topology and employing Linear Technology Corporation's advanced bipolar complementary processing. For a single amplifier version of the LT1358/LT1359 see the LT1357 data sheet. For higher bandwidth devices with higher supply currents see the LT1360 through LT1365 data sheets. For lower supply current amplifiers see the LT1354 and LT1355/LT1356 data sheets. Singles, duals, and quads of each amplifier are available.

TYPICAL APPLICATION

DAC I-to-V Converter



A_V = –1 Large-Signal Response

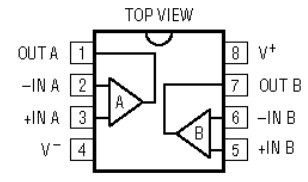


ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 36V
Differential Input Voltage
(Transient Only) (Note 2) ..... ±10V
Input Voltage ..... $\pm V_S$
Output Short-Circuit Duration (Note 3) ..... Indefinite

Operating Temperature Range (Note 7) ...–40°C to 85°C
Specified Temperature Range (Note 8) ....–40°C to 85°C
Maximum Junction Temperature (See Below)
Plastic Package ..... 150°C
Storage Temperature Range .....–65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

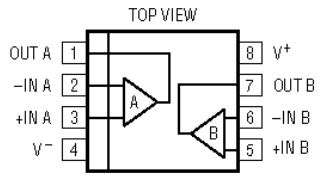
PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PDIP

T_{JMAX} = 150°C, θ_{JA} = 130°C/W

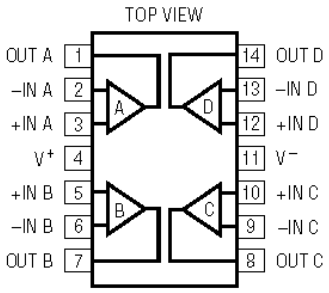
ORDER PART NUMBER
LT1358CN8



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 190°C/W

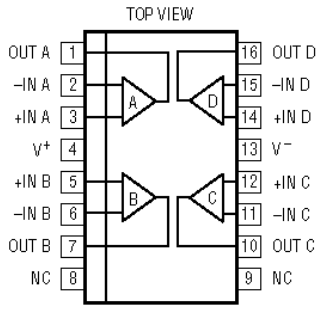
ORDER PART NUMBER
LT1358CS8
S8 PART MARKING
1358



N PACKAGE
14-LEAD PDIP

T_{JMAX} = 150°C, θ_{JA} = 110°C/W

ORDER PART NUMBER
LT1359CN



S PACKAGE
16-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LT1359CS

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		±15V		0.2	0.6	mV
			±5V		0.2	0.6	mV
			±2.5V		0.3	0.8	mV
I_{OS}	Input Offset Current		±2.5V to ±15V		40	120	nA
I_B	Input Bias Current		±2.5V to ±15V		120	500	nA
e_n	Input Noise Voltage	f = 10kHz	±2.5V to ±15V		8		$nV/\sqrt{Hz}$
i_n	Input Noise Current	f = 10kHz	±2.5V to ±15V		0.8		$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	V_{CM} = ±12V	±15V	35	80		MΩ
	Input Resistance	Differential	±15V		6		MΩ
C_{IN}	Input Capacitance		±15V		3		pF

ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
	Input Voltage Range$^+$		±15V	12.0	13.4		V
			±5V	2.5	3.5		V
			±2.5V	0.5	1.1		V
	Input Voltage Range$^-$		±15V		–13.2	–12.0	V
			±5V		–3.3	–2.5	V
			±2.5V		–0.9	–0.5	V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±12V	±15V	83	97		dB
		V_{CM} = ±2.5V	±5V	78	84		dB
		V_{CM} = ±0.5V	±2.5V	68	75		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.5V to ±15V		92	106		dB
A_{VOL}	Large-Signal Voltage Gain	V_{OUT} = ±12V, R_L = 1k	±15V	20	65		V/mV
		V_{OUT} = ±10V, R_L = 500Ω	±15V	7	25		V/mV
		V_{OUT} = ±2.5V, R_L = 1k	±5V	20	45		V/mV
		V_{OUT} = ±2.5V, R_L = 500Ω	±5V	7	25		V/mV
		V_{OUT} = ±2.5V, R_L = 150Ω	±5V	1.5	6		V/mV
		V_{OUT} = ±1V, R_L = 500Ω	±2.5V	7	30		V/mV
V_{OUT}	Output Swing	R_L = 1k, V_{IN} = ±40mV	±15V	13.3	13.8		±V
		R_L = 500Ω, V_{IN} = ±40mV	±15V	12.5	13.0		±V
		R_L = 500Ω, V_{IN} = ±40mV	±5V	3.5	4.0		±V
		R_L = 150Ω, V_{IN} = ±40mV	±5V	3.0	3.3		±V
		R_L = 500Ω, V_{IN} = ±40mV	±2.5V	1.3	1.7		±V
I_{OUT}	Output Current	V_{OUT} = ±12.5V	±15V	25	30		mA
		V_{OUT} = ±3V	±5V	20	25		mA
I_{SC}	Short-Circuit Current	V_{OUT} = 0V, V_{IN} = ±3V	±15V	30	42		mA
SR	Slew Rate	A_V = –2, (Note 4)	±15V	300	600		V/µs
			±5V	150	220		V/µs
	Full Power Bandwidth	10V Peak, (Note 5)	±15V		9.6		MHz
		3V Peak, (Note 5)	±5V		11.7		MHz
GBW	Gain Bandwidth	f = 200kHz, R_L = 2k	±15V	18	25		MHz
			±5V	15	22		MHz
			±2.5V		20		MHz
t_r, t_f	Rise Time, Fall Time	A_V = 1, 10%-90%, 0.1V	±15V		8		ns
			±5V		9		ns
	Overshoot	A_V = 1, 0.1V	±15V		27		%
			±5V		27		%
	Propagation Delay	50% V_{IN} to 50% V_{OUT}, 0.1V	±15V		9		ns
			±5V		11		ns
t_s	Settling Time	10V Step, 0.1%, A_V = –1	±15V		115		ns
		10V Step, 0.01%, A_V = –1	±15V		220		ns
		5V Step, 0.1%, A_V = –1	±5V		110		ns
		5V Step, 0.01%, A_V = –1	±5V		380		ns
	Differential Gain	f = 3.58MHz, A_V = 2, R_L = 1k	±15V		0.1		%
			±5V		0.1		%
	Differential Phase	f = 3.58MHz, A_V = 2, R_L = 1k	±15V		0.50		Deg
			±5V		0.35		Deg
R_O	Output Resistance	A_V = 1, f = 100kHz	±15V		0.3		Ω
	Channel Separation	V_{OUT} = ±10V, R_L = 500Ω	±15V	100	113		dB
I_S	Supply Current	Each Amplifier	±15V		2.0	2.5	mA
		Each Amplifier	±5V		1.9	2.4	mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the temperature range $-40°C \le T_A \le 85°C$, $V_{CM} = 0V$ unless otherwise noted. (Note 8)

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm12V$, $R_L = 1k$	±15V	●	10.0			V/mV
		$V_{OUT} = \pm10V$, $R_L = 500\Omega$	±15V	●	2.5			V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 1k$	±5V	●	10.0			V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 500\Omega$	±5V	●	2.5			V/mV
		$V_{OUT} = \pm2.5V$, $R_L = 150\Omega$	±5V	●	0.6			V/mV
		$V_{OUT} = \pm1V$, $R_L = 500\Omega$	±2.5V	●	2.5			V/mV
V_{OUT}	Output Swing	$R_L = 1k$, $V_{IN} = \pm40mV$	±15V	●	13.0			±V
		$R_L = 500\Omega$, $V_{IN} = \pm40mV$	±15V	●	12.0			±V
		$R_L = 500\Omega$, $V_{IN} = \pm40mV$	±5V	●	3.4			±V
		$R_L = 150\Omega$, $V_{IN} = \pm40mV$	±5V	●	2.6			±V
		$R_L = 500\Omega$, $V_{IN} = \pm40mV$	±2.5V	●	1.2			±V
I_{OUT}	Output Current	$V_{OUT} = \pm12V$	±15V	●	24.0			mA
		$V_{OUT} = \pm2.6V$	±5V	●	17.3			mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = \pm3V$	±15V	●	24			mA
SR	Slew Rate	$A_V = -2$, (Note 4)	±15V	●	180			V/µs
			±5V	●	100			V/µs
GBW	Gain Bandwidth	f = 200kHz, $R_L = 2k$	±15V	●	14			MHz
			±5V	●	11			MHz
	Channel Separation	$V_{OUT} = \pm10V$, $R_L = 500\Omega$	±15V	●	98			dB
I_S	Supply Current	Each Amplifier	±15V	●			3.0	mA
		Each Amplifier	±5V	●			2.9	mA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Differential inputs of ±10V are appropriate for transient operation only, such as during slewing. Large, sustained differential inputs will cause excessive power dissipation and may damage the part. See Input Considerations in the Applications Information section of this data sheet for more details.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 4: Slew rate is measured between ±10V on the output with ±6V input for ±15V supplies and ±1V on the output with ±1.75V input for ±5V supplies.

Note 5: Full power bandwidth is calculated from the slew rate measurement: $FPBW = (SR)/2\pi V_P$.

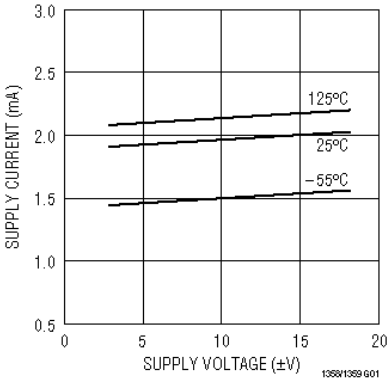
Note 6: This parameter is not 100% tested.

Note 7. The LT1358C/LT1359C are guaranteed functional over the operating temperature range of –40°C to 85°C.

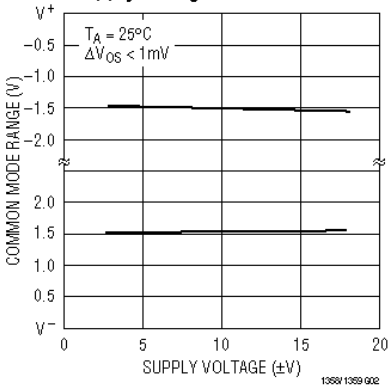
Note 8: The LT1358C/LT1359C are guaranteed to meet specified performance from 0°C to 70°C. The LT1358C/LT1359C are designed, characterized and expected to meet specified performance from –40°C to 85°C, but are not tested or QA sampled at these temperatures. For guaranteed I-grade parts, consult the factory.

TYPICAL PERFORMANCE CHARACTERISTICS

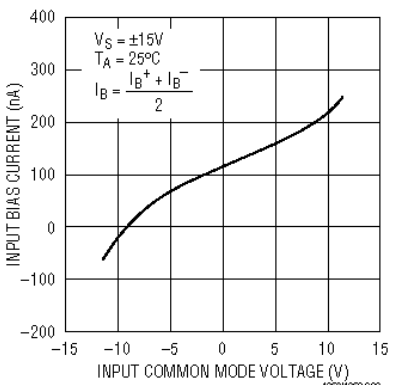
Supply Current vs Supply Voltage and Temperature



Input Common Mode Range vs Supply Voltage

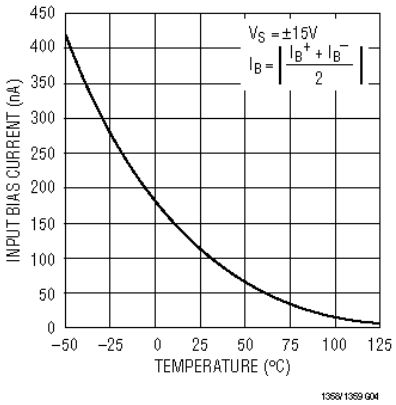


Input Bias Current vs Input Common Mode Voltage



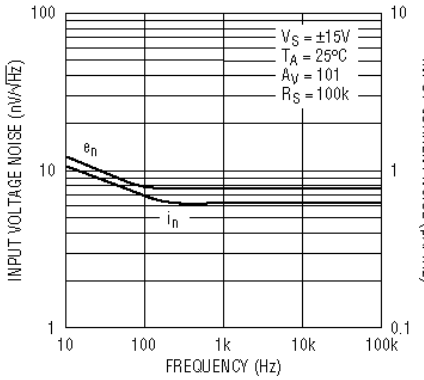
TYPICAL PERFORMANCE CHARACTERISTICS

Input Bias Current vs Temperature



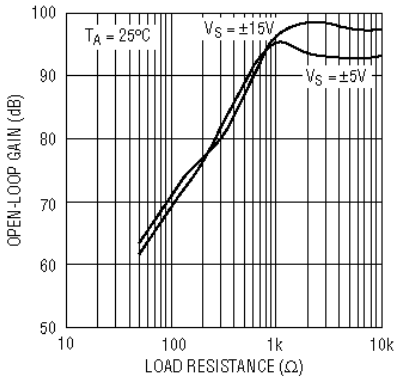
1358/1359 G04

Input Noise Spectral Density



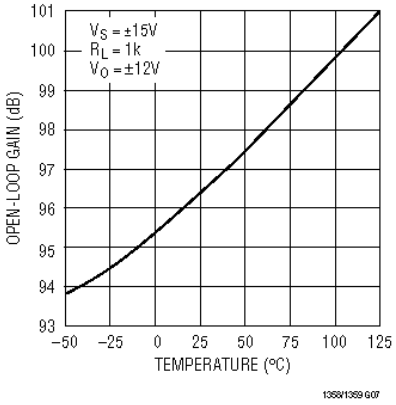
1358/1359 G05

Open-Loop Gain vs Resistive Load



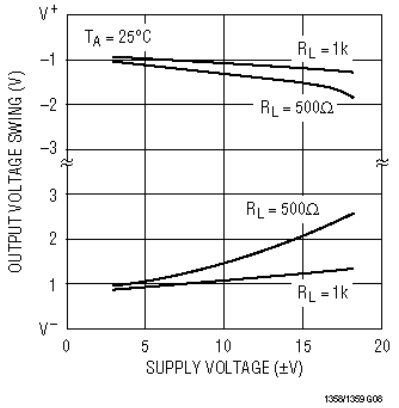
1358/1359 G06

Open-Loop Gain vs Temperature



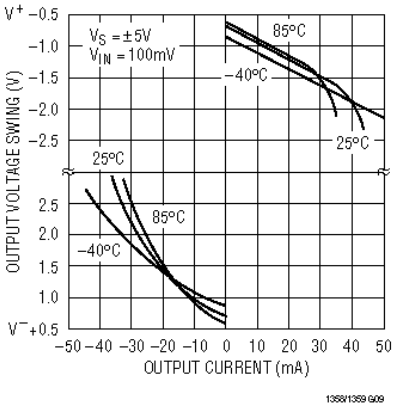
1358/1359 G07

Output Voltage Swing vs Supply Voltage



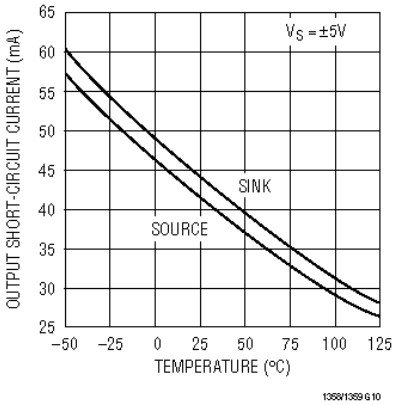
1358/1359 G08

Output Voltage Swing vs Load Current



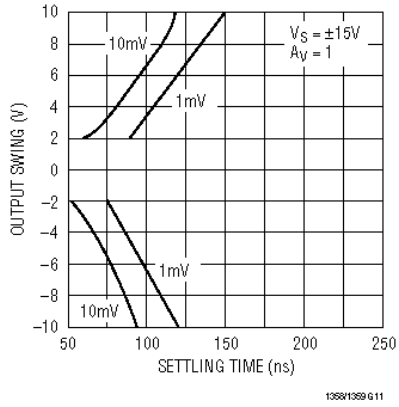
1358/1359 G09

Output Short-Circuit Current vs Temperature



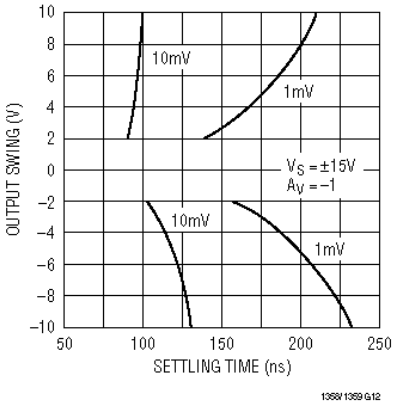
1358/1359 G10

Settling Time vs Output Step (Noninverting)



1358/1359 G11

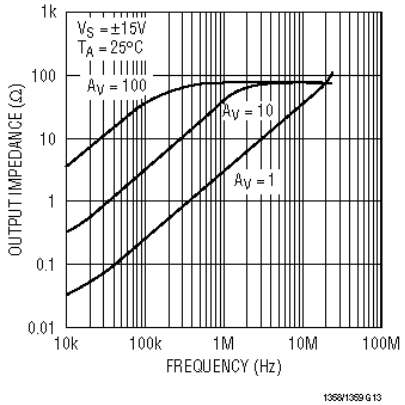
Settling Time vs Output Step (Inverting)



1358/1359 G12

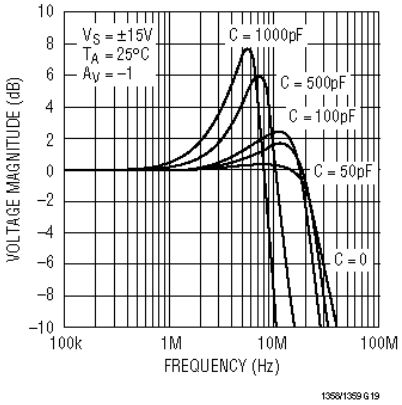
TYPICAL PERFORMANCE CHARACTERISTICS

Output Impedance vs Frequency



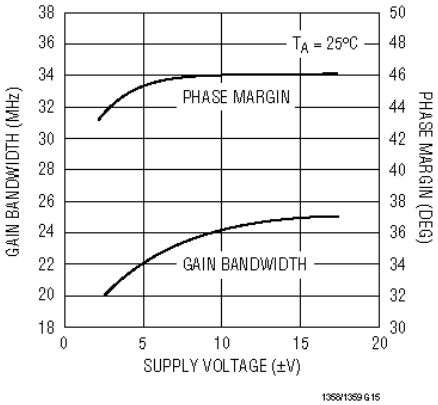
1358/1359 G13

Frequency Response vs Capacitive Load



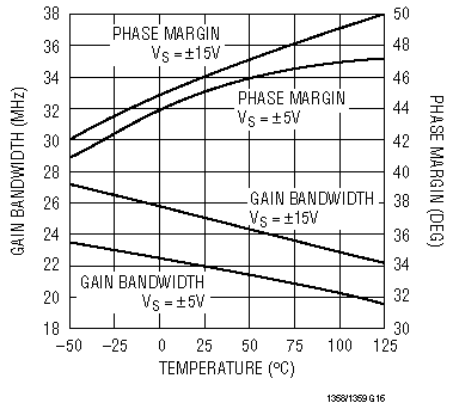
1358/1359 G19

Gain Bandwidth and Phase Margin vs Supply Voltage



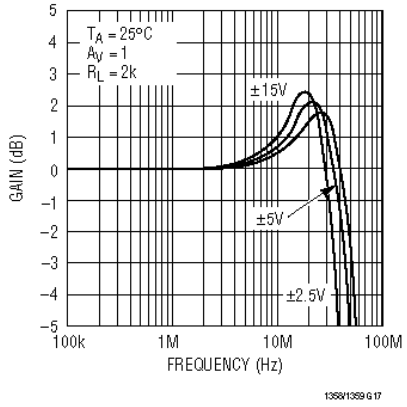
1358/1359 G15

Gain Bandwidth and Phase Margin vs Temperature



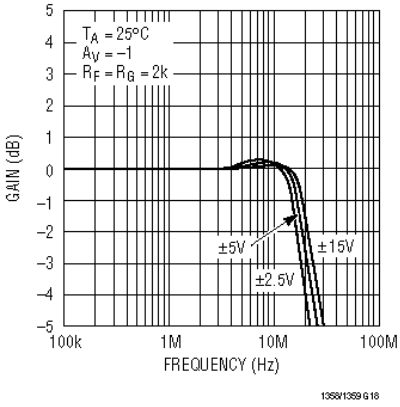
1358/1359 G16

Frequency Response vs Supply Voltage ($A_V = 1$)



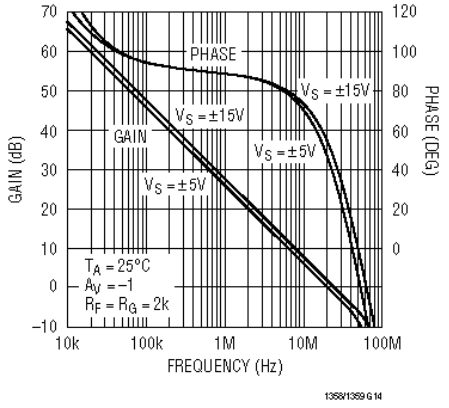
1358/1359 G17

Frequency Response vs Supply Voltage ($A_V = -1$)



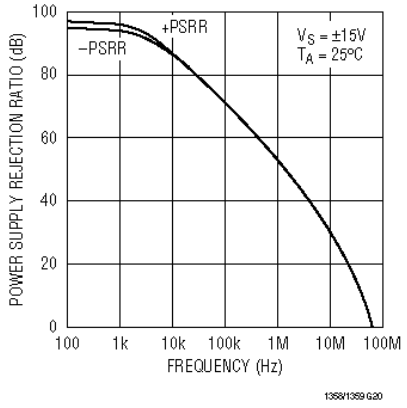
1358/1359 G18

Gain and Phase vs Frequency



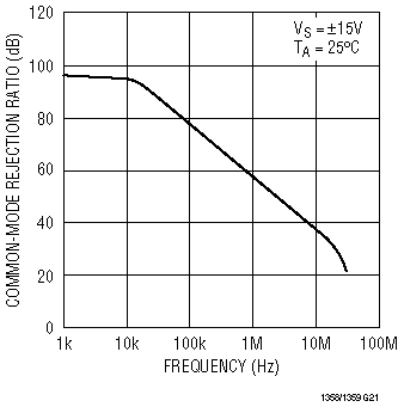
1358/1359 G14

Power Supply Rejection Ratio vs Frequency



1358/1359 G20

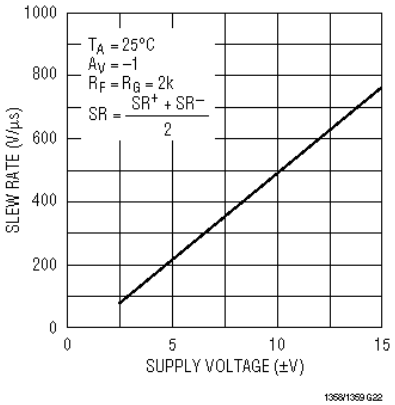
Common Mode Rejection Ratio vs Frequency



1358/1359 G21

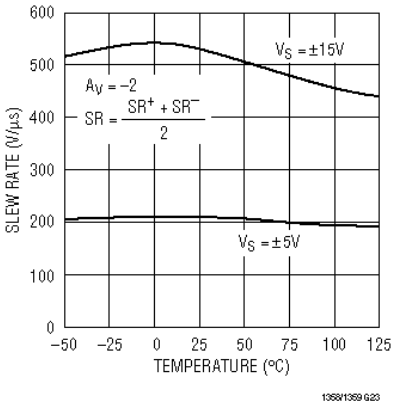
TYPICAL PERFORMANCE CHARACTERISTICS

Slew Rate vs Supply Voltage



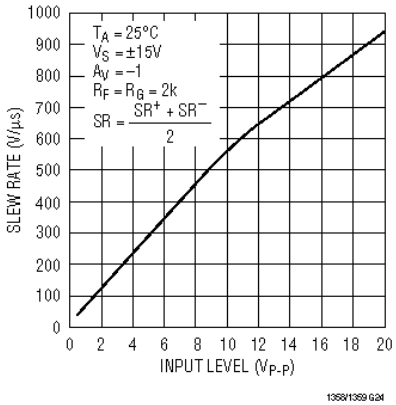
1358/1359 G22

Slew Rate vs Temperature



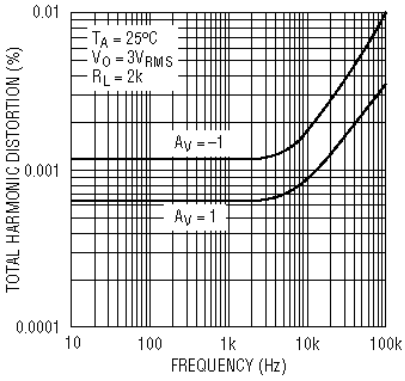
1358/1359 G23

Slew Rate vs Input Level



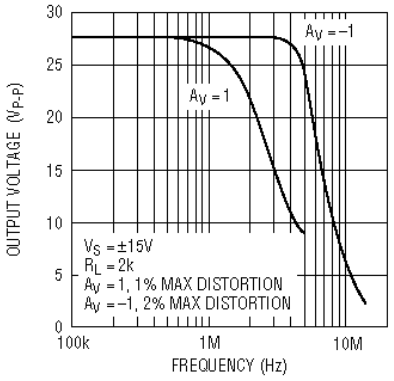
1358/1359 G24

Total Harmonic Distortion vs Frequency



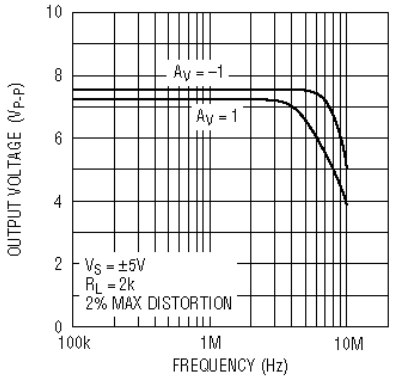
1358/1359 G25

Undistorted Output Swing vs Frequency (±15V)



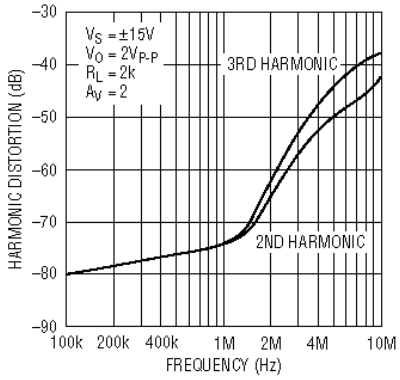
1358/1359 G26

Undistorted Output Swing vs Frequency (±5V)



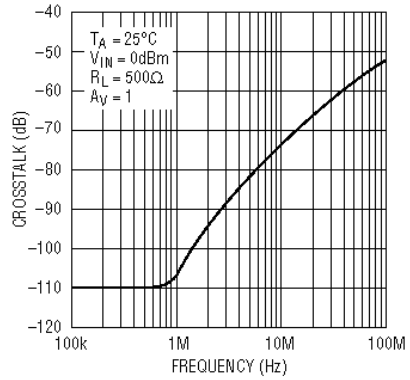
1358/1359 G27

2nd and 3rd Harmonic Distortion vs Frequency



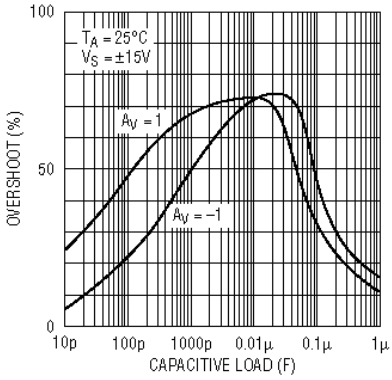
1358/1359 G28

Crosstalk vs Frequency



1358/1359 G29

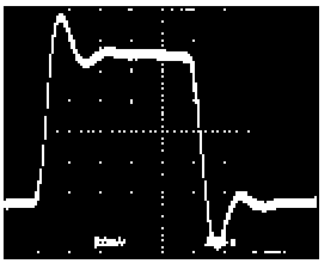
Capacitive Load Handling



1358/1359 G30

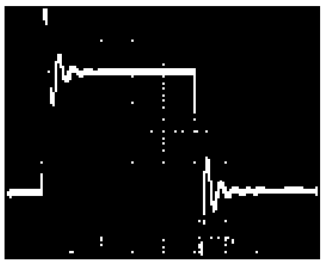
TYPICAL PERFORMANCE CHARACTERISTICS

Small-Signal Transient
($A_V = 1$)



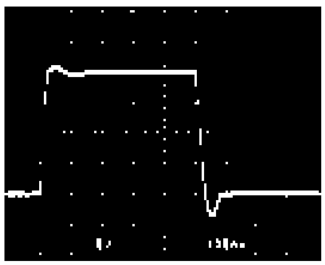
Small-Signal Transient
($A_V = -1$)

Small-Signal Transient
($A_V = -1$, $C_L = 1000pF$)



Large-Signal Transient
($A_V = 1$)

Large-Signal Transient
($A_V = -1$)



Large-Signal Transient
($A_V = 1$, $C_L = 10,000pF$)

APPLICATIONS INFORMATION

Layout and Passive Components

The LT1358/LT1359 amplifiers are easy to use and tolerant of less than ideal layouts. For maximum performance (for example, fast 0.01% settling) use a ground plane, short lead lengths, and RF-quality bypass capacitors (0.01µF to 0.1µF). For high drive current applications use low ESR bypass capacitors (1µF to 10µF tantalum).

The parallel combination of the feedback resistor and gain setting resistor on the inverting input combine with the input capacitance to form a pole which can cause peaking or oscillations. If feedback resistors greater than 5k are used, a parallel capacitor of value

$$C_F > R_G \times C_{IN} / R_F$$

should be used to cancel the input pole and optimize dynamic performance. For unity-gain applications where a large feedback resistor is used, C_F should be greater than or equal to C_{IN}.

Capacitive Loading

The LT1358/LT1359 are stable with any capacitive load. As the capacitive load increases, both the bandwidth and phase margin decrease so there will be peaking in the frequency domain and in the transient response. Coaxial cable can be driven directly, but for best pulse fidelity a resistor of value equal to the characteristic impedance of the cable (i.e., 75Ω) should be placed in series with the output. The other end of the cable should be terminated with the same value resistor to ground.

Input Considerations

Each of the LT1358/LT1359 inputs is the base of an NPN and a PNP transistor whose base currents are of opposite polarity and provide first-order bias current cancellation.