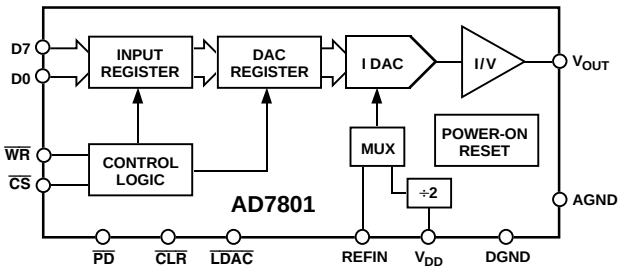
+2.7 V to +5.5 V, Parallel Input, Voltage Output 8-Bit DAC

AD7801

FEATURES
Single 8-Bit DAC
20-Pin SOIC/TSSOP Package
+2.7 V to +5.5 V Operation
Internal and External Reference Capability
DAC Power-Down Function
Parallel Interface
On-Chip Output Buffer Rail-to-Rail Operation
Low Power Operation 1.75 mA max @ 3.3 V
Power-Down to 1 μA max @ 25°C

APPLICATIONS
Portable Battery Powered Instruments
Digital Gain and Offset Adjustment
Programmable Voltage and Current Sources
Programmable Attenuators

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7801 is a single, 8-bit, voltage out DAC that operates from a single +2.7 V to +5.5 V supply. Its on-chip precision output buffer allows the DAC output to swing rail to rail. The AD7801 has a parallel microprocessor and DSP compatible interface with high speed registers and double buffered interface logic. Data is loaded to the input register on the rising edge of $\overline{CS}$ or $\overline{WR}$.

Reference selection for the AD7801 can be either an internal reference derived from the V_{DD} or an external reference applied at the REFIN pin. The output of the DAC can be cleared by using the asynchronous $\overline{CLR}$ input.

The low power consumption of this part makes it ideally suited to portable battery operated equipment. The power consumption is less than 5 mW at 3.3 V, reducing to less than 3 μW in power-down mode.

The AD7801 is available in a 20-lead SOIC and a 20-lead TSSOP package.

PRODUCT HIGHLIGHTS

1. Low Power, Single Supply operation. This part operates from a single +2.7 V to +5.5 V supply and consumes typically 5 mW at 3 V, making it ideal for battery powered applications.
2. The on-chip output buffer amplifier allows the output of the DAC to swing rail to rail with a settling time of typically 1.2 μs.
3. Internal or external reference capability.
4. High speed parallel interface.
5. Power-down capability. When powered down the DAC consumes less than 1 μA at 25°C.
6. Packaged in 20-lead SOIC and TSSOP packages.

REV. 0

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AD7801–SPECIFICATIONS

(V_{DD} = +2.7 V to +5.5 V, Internal Reference; C_L = 100 pF, R_L = 10 kΩ to V_{DD} and GND. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	B Versions[1]	Units	Conditions/Comments
STATIC PERFORMANCE			
Resolution	8	Bits	
Relative Accuracy[2]	±1	LSB max	
Differential Nonlinearity	±1	LSB max	Guaranteed Monotonic
Zero-Code Error @ +25°C	3	LSB typ	All Zeros Loaded to DAC Register
Full-Scale Error	–0.75	LSB typ	All Ones Loaded to DAC Register
Zero-Code Error Drift	100	µV/°C typ	
Gain Error[3]	±1	% FSR typ	
DAC REFERENCE INPUT			
REFIN Input Range	1 to V_{DD}/2	V min/V max	
REFIN Input Impedance	10	MΩ typ	
OUTPUT CHARACTERISTICS			
Output Voltage Range	0 to V_{DD}	V min/V max	
Output Voltage Settling Time	2	µs max	Typically 1.2 µs
Slew Rate	7.5	V/µs typ	
Digital-to-Analog Glitch Impulse	1	nV-s typ	1 LSB Change Around Major Carry
Digital Feedthrough	0.2	nV-s typ	
DC Output Impedance	40	Ω typ	
Short Circuit Current	14	mA typ	
Power Supply Rejection Ratio[4]	0.0003	%/% max	ΔV_{DD} = ±10%
LOGIC INPUTS			
Input Current	±10	µA max	
V_{INL}, Input Low Voltage	0.8	V max	V_{DD} = +5 V
V_{INL}, Input Low Voltage	0.6	V max	V_{DD} = +3 V
V_{INH}, Input High Voltage	2.4	V min	V_{DD} = +5 V
V_{INH}, Input High Voltage	2.1	V min	V_{DD} = +3 V
Pin Capacitance	7	pF max	
POWER REQUIREMENTS			
V_{DD}	2.7/5.5	V min/V max	
I_{DD} (Normal Mode)			DAC Active and Excluding Load Current
V_{DD} = 3.3 V			V_{IH} = V_{DD} and V_{IL} = GND
@ 25°C	1.55	mA max	See Figure 6
T_{MIN} to T_{MAX}	1.75	mA max	
V_{DD} = 5.5 V			
@ 25°C	2.35	mA max	
T_{MIN} to T_{MAX}	2.5	mA max	
I_{DD} (Power-Down)			
@ 25°C	1	µA max	V_{IH} = V_{DD} and V_{IL} = GND
T_{MIN} to T_{MAX}	2	µA max	See Figure 18

NOTES
[1]Temperature ranges are as follows: B Version: –40°C to +105°C
[2]Relative Accuracy is calculated using a reduced code range of 15 to 245.
[3]Gain Error is specified between Codes 15 and 245. The actual error at Code 15 is typically 3 LSB.
[4]Guaranteed by characterization at product release, not production tested.

Specifications subject to change without notice.

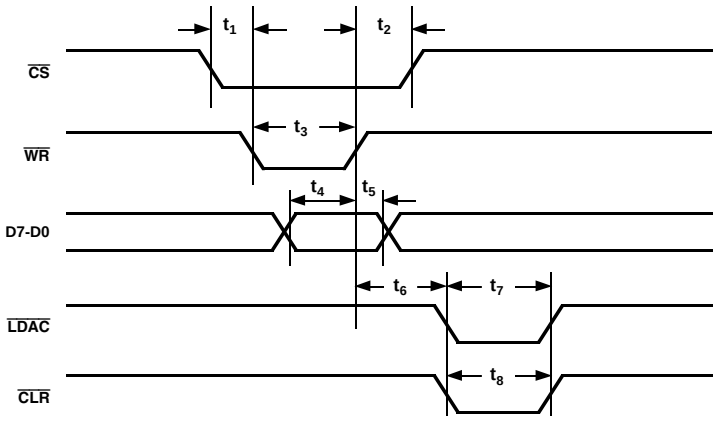


Figure 1. Timing Diagram for Parallel Data Write

TIMING CHARACTERISTICS[1, 2]

(V_{DD} = +2.7 V to +5.5 V; GND = 0 V; Internal V_{DD}/2 Reference. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX} (B Version)	Units	Conditions/Comments
t_1	0	ns min	Chip Select to Write Setup Time
t_2	0	ns min	Chip Select to Write Hold Time
t_3	20	ns min	Write Pulse Width
t_4	15	ns min	Data Setup Time
t_5	4.5	ns min	Data Hold Time
t_6	20	ns min	Write to $\overline{\text{LDAC}}$ Setup Time
t_7	20	ns min	$\overline{\text{LDAC}}$ Pulse Width
t_8	20	ns min	$\overline{\text{CLR}}$ Pulse Width

NOTES
[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. tr and tf should not exceed 1 µs on any digital input.
[2]See Figure 1.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to GND ..... –0.3 V to +7 V
Reference Input Voltage to AGND ....–0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND .....–0.3 V to V_{DD} + 0.3 V
AGND to DGND .....–0.3 V to +0.3 V
V_{OUT} to AGND ..... –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
  Commercial (B Version) ..... –40°C to +105°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature .....+150°C
SSOP Package, Power Dissipation ..... 700 mW
  θ_{JA} Thermal Impedance ..... 143°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) .....+215°C
    Infrared (15 sec) .....+220°C
SOIC Package, Power Dissipation ..... 870 mW
  θ_{JA} Thermal Impedance ..... 74°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) .....+215°C
    Infrared (15 sec) .....+220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

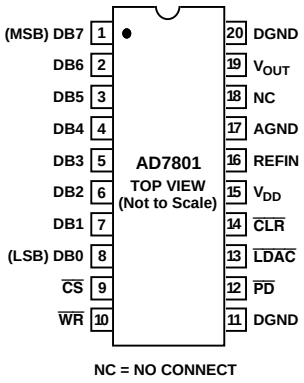
Model	Temperature Range	Package Option*
AD7801BR	–40°C to +105°C	R-20
AD7801BRU	–40°C to +105°C	RU-20

*R = Small Outline; RU = Thin Shrink Small Outline.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7801 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1–8	D7–D0	Parallel Data Inputs. 8-bit data is loaded to the input register of the AD7801 under the control of $\overline{CS}$ and $\overline{WR}$.
9	$\overline{CS}$	Chip Select. Active low logic input.
10	$\overline{WR}$	Write Input. $\overline{WR}$ is an active low logic input used in conjunction with $\overline{CS}$ to write data to the input register.
11	DGND	Digital Ground
12	$\overline{PD}$	Active low input used to put the part into low power mode reducing current consumption to less than 1 μA.
13	$\overline{LDAC}$	Load DAC Logic Input. When this logic input is taken low the DAC output is updated with the contents of its DAC register. If $\overline{LDAC}$ is permanently tied low the DAC is updated on the rising edge of $\overline{WR}$.
14	$\overline{CLR}$	Asynchronous Clear Input (Active Low). When this input is taken low the DAC register is loaded with all zeroes and the DAC output is cleared to zero volts.
15	V_{DD}	Power Supply Input. This part can be operated from +2.7 V to +5.5 V and should be decoupled to GND.
16	REFIN	External Reference Input. This can be used as the reference for the DAC. The range on this reference input is 1 V to $V_{DD}/2$. If REFIN is tied directly to V_{DD} the internal $V_{DD}/2$ reference is selected.
17	AGND	Analog Ground reference point and return point for all analog current on the part.
18	NC	No Connect Pin.
19	V_{OUT}	Analog Output Voltage from the DAC. The output amplifier can swing rail to rail on its output.
20	DGND	Digital Ground reference point and return point for all digital current on the part.

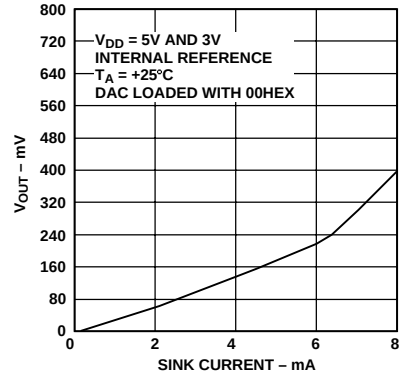


Figure 2. Output Sink Current Capability with V_{DD} = 3 V and V_{DD} = 5 V

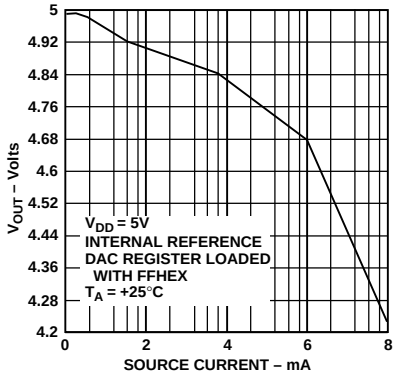


Figure 3. Output Source Current Capability with V_{DD} = 5 V

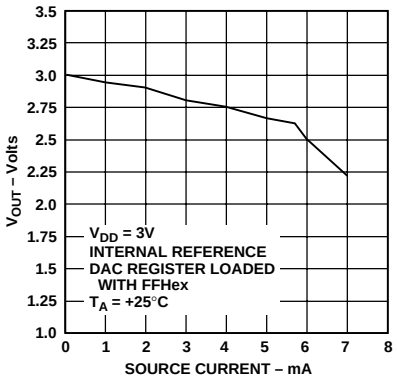


Figure 4. Output Source Current Capability with V_{DD} = 3 V

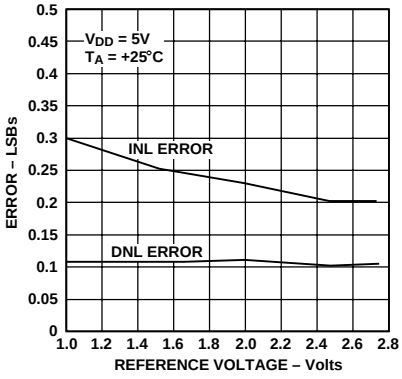


Figure 5. Relative Accuracy vs. External Reference

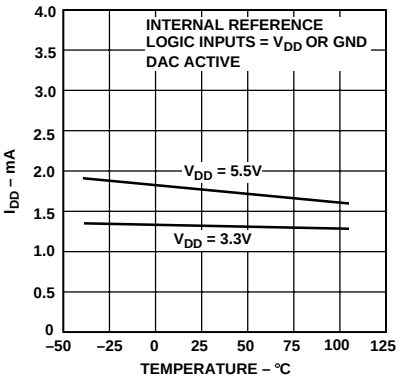


Figure 6. Typical Supply Current vs. Temperature

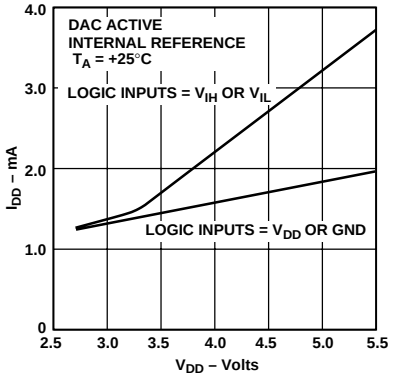


Figure 7. Typical Supply Current vs. Supply Voltage

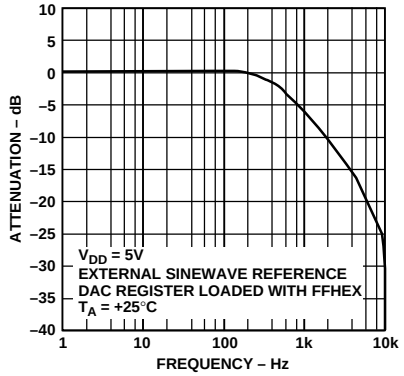


Figure 8. Large Scale Signal Frequency Response

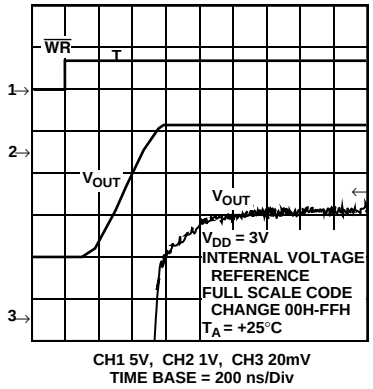


Figure 9. Full-Scale Settling Time

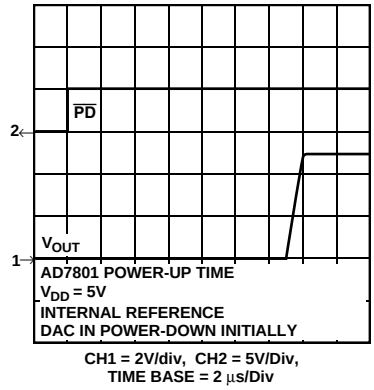


Figure 10. Exiting Power-Down (Full Power-Down)

AD7801–Typical Performance Characteristics

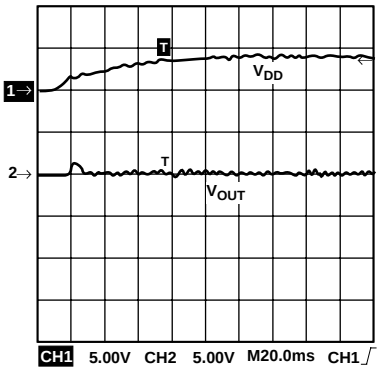


Figure 11. Power-On—Reset

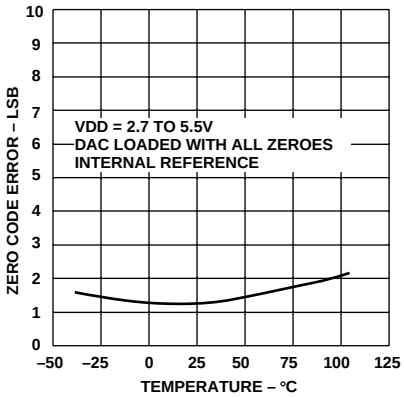


Figure 12. Zero Code Error vs. Temperature

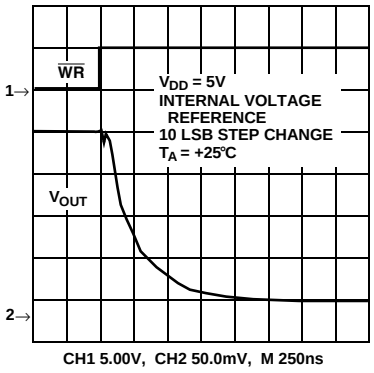


Figure 13. Small-Scale Settling Time

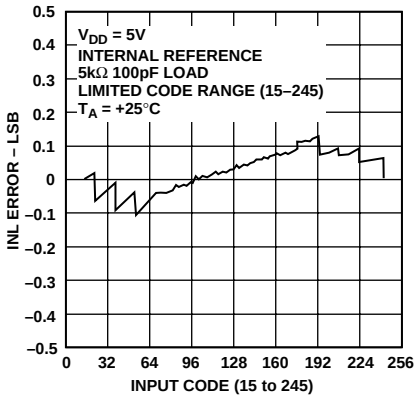


Figure 14. Integral Linearity Plot

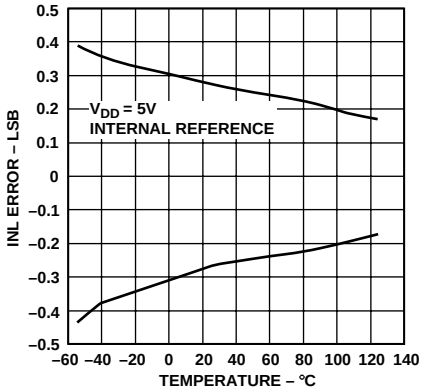


Figure 15. Typical INL vs. Temperature

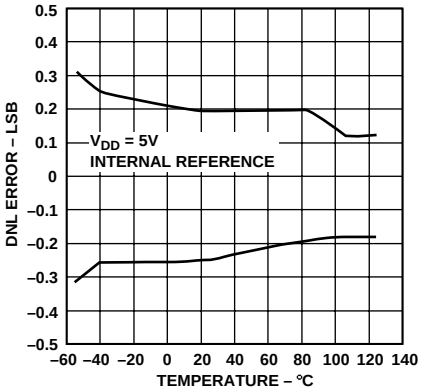


Figure 16. Typical DNL vs. Temperature

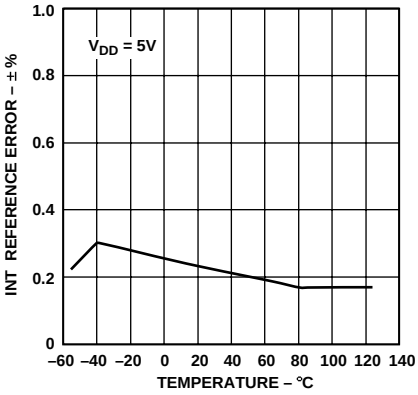


Figure 17. Typical Internal Reference Error vs. Temperature

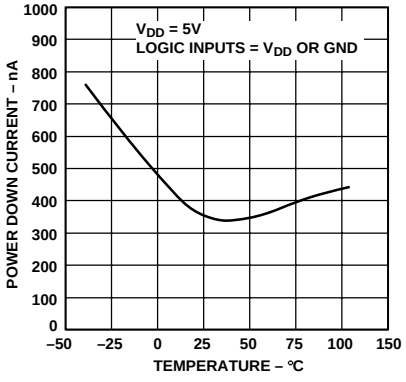


Figure 18. Power-Down Current vs. Temperature

TERMINOLOGY

Integral Nonlinearity

For the DAC, Relative Accuracy or End-Point nonlinearity is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A graphical representation of the transfer curve is shown in Figure 14.

Differential Nonlinearity

Differential Nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity.

Zero-Code Error

Zero-Code Error is the measured output voltage from V_{OUT} of the DAC when zero code (all zeros) is loaded to the DAC latch. It is due to a combination of the offset errors in the DAC and output amplifier. Zero-code error is expressed in LSBs.

Gain Error

This is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from ideal expressed as a percent of the full-scale value. It includes full-scale errors but not offset errors.

Digital-to-Analog Glitch Impulse

Digital-to-Analog Glitch Impulse is the impulse injected into the analog output when the digital inputs change state with the DAC selected and the $\overline{\text{LDAC}}$ used to update the DAC. It is normally specified as the area of the glitch in nV-secs and measured when the digital input code is changed by 1 LSB at the major carry transition.

Digital Feedthrough

Digital Feedthrough is a measure of the impulse injected into the analog output of a DAC from the digital inputs of the same DAC, but is measured when the DAC is not updated. It is specified in nV-secs and measured with a full-scale code change on the data bus, i.e., from all 0s to all 1s and vice versa.

Power Supply Rejection Ratio (PSRR)

This specification indicates how the output of the DAC is affected by changes in the power supply voltage. Power supply rejection ratio is quoted in terms of % change in output per % change in V_{DD} for full-scale output of the DAC. V_{DD} is varied ±10%.

GENERAL DESCRIPTION

D/A Section

The AD7801 is an 8-bit voltage output digital-to-analog converter. The architecture consists of a reference amplifier and a current source DAC followed by a current-to-voltage converter capable of generating rail-to-rail voltages on the output of the DAC. Figure 19 shows a block diagram of the basic DAC architecture.

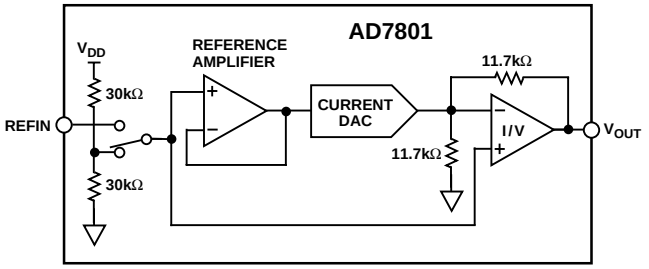


Figure 19. DAC Architecture

The DAC output is internally buffered and has rail-to-rail output characteristics. The output amplifier is capable of driving a load of 100 pF and 10 kΩ to both V_{DD} and ground. The reference selection for the DAC can be either internally generated from V_{DD} or externally applied through the REFIN pin. A comparator on the REFIN pin detects whether the required reference is the internally generated reference or the externally applied voltage to the REFIN pin. If REFIN is connected to V_{DD}, the reference selected is the internally generated $V_{DD}/2$ reference. When an externally applied voltage is more than one volt below V_{DD}, the comparator selection switches to the externally applied voltage on the REFIN pin. The range on the external reference input is from 1.0 V to $V_{DD}/2$ V. The output voltage from the DAC is given by:

$$V_O = 2V_{REF} \times \left(\frac{N}{256}\right)$$

where V_{REF} is the voltage applied to the external REFIN pin or $V_{DD}/2$ when the internal reference is selected. N is the decimal equivalent of the code loaded to the DAC register and ranges from 0 to 255.

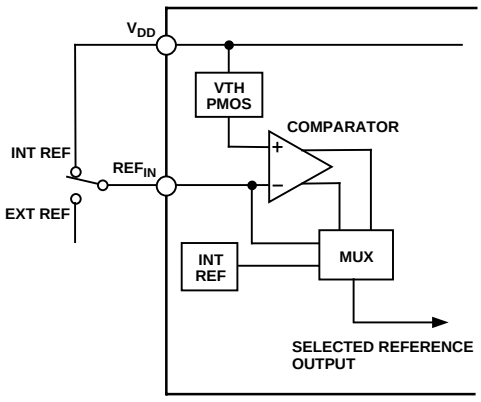


Figure 20. Reference Selection Circuitry

Reference

The AD7801 has the ability to use either an external reference applied through the REFIN pin or an internal reference generated from V_{DD}. Figure 20 shows the reference input arrangement where either the internal $V_{DD}/2$ or the externally applied reference can be selected.

The internal reference is selected by tying the REFIN pin to V_{DD}. If an external reference is to be used, this can be directly applied to the REFIN pin and if this is 1 V below V_{DD}, the internal circuitry will select this externally applied reference as the reference source for the DAC.

Digital Interface

The AD7801 contains a fast parallel interface allowing this DAC to interface to industry standard microprocessors, microcontrollers and DSP machines. There are two modes in which this parallel interface can be configured to update the DAC output. The synchronous update mode allows synchronous updating of the DAC output; the automatic update mode allows the DAC to be updated individually following a write cycle. Figure 21 shows the internal logic associated with the digital interface. The PON STRB signal is internally generated from the power-on reset circuitry and is low during the power-on reset phase of the power up procedure.

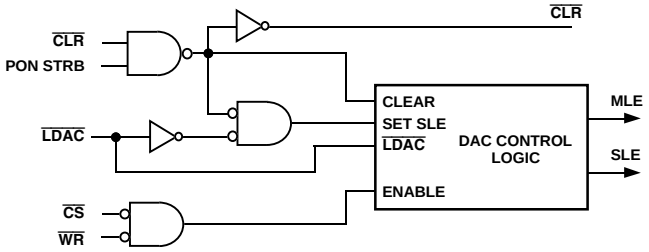


Figure 21. Logic Interface

The AD7801 has a double buffered interface, which allows for synchronous updating of the DAC output. Figure 22 shows a block diagram of the register arrangement within the AD7801.

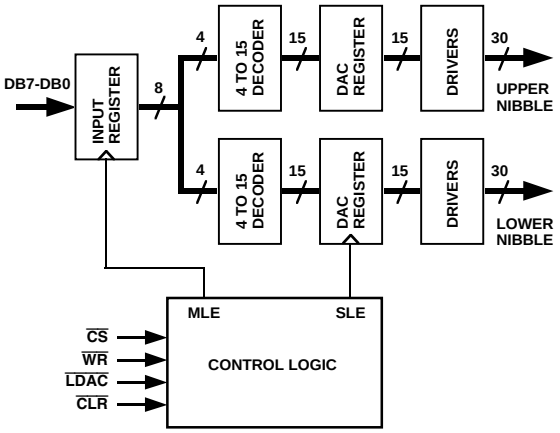


Figure 22. Register Arrangement

Automatic Update Mode

In this mode of operation the $\overline{LDAC}$ signal is permanently tied low. The state of the $\overline{LDAC}$ is sampled on the rising edge of $\overline{WR}$. $\overline{LDAC}$ being low allows the DAC register to be automatically updated on the rising edge of $\overline{WR}$. The output update occurs on the rising edge of $\overline{WR}$. Figure 23 shows the timing associated with the automatic update mode of operation and also the status of the various registers during this frame.

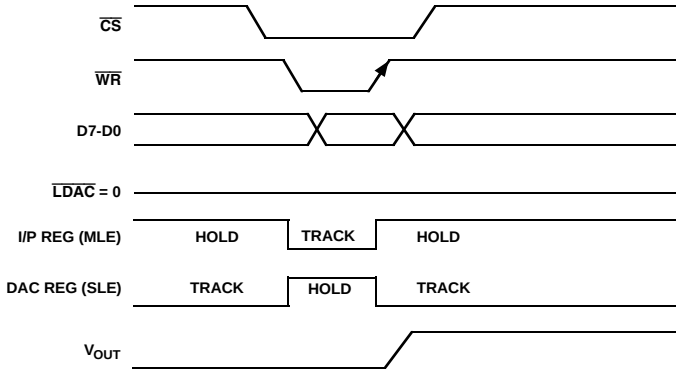


Figure 23. Timing and Register Arrangement for Automatic Update Mode

Synchronous Update Mode

In this mode of operation the $\overline{LDAC}$ signal is used to update the DAC output to synchronize with other updates in the system. The state of the $\overline{LDAC}$ is sampled on the rising edge of $\overline{WR}$. If $\overline{LDAC}$ is high, the automatic update mode is disabled and the DAC latch is updated at any time after the write by taking $\overline{LDAC}$ low. The output update occurs on the falling edge of $\overline{LDAC}$. $\overline{LDAC}$ must be taken back high again before the next data transfer takes place. Figure 24 shows the timing associated with the synchronous update mode of operation and also the status of the various registers during this frame.

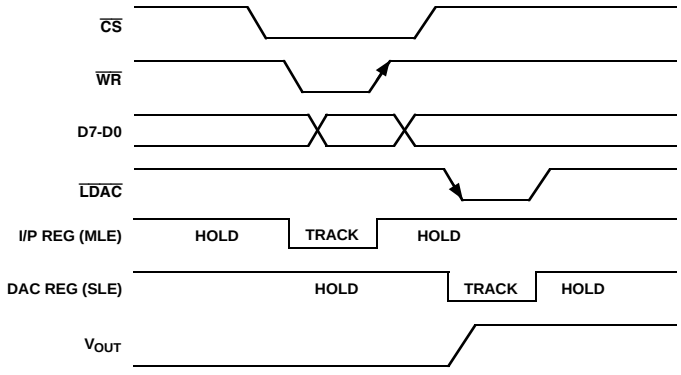


Figure 24. Timing and Register Arrangement for Synchronous Update Mode

POWER-ON RESET

The AD7801 has a power-on reset circuit designed to allow output stability during power up. This circuit holds the DAC in a reset state until a write takes place to the DAC. In the reset state all zeros are latched into the input register of the DAC and the DAC register is in transparent mode thus the output of the DAC is held at ground potential until a write takes place to the DAC. The power-on reset circuitry generates a PON STRB signal which is a gating signal used within the logic to identify a power-on condition.

POWER-DOWN FEATURES

The AD7801 has a power-down feature implemented by exercising the external $\overline{PD}$ pin. An active low signal puts the complete DAC into power-down mode. When in power-down, the current consumption of the device is reduced to less than 1 μA max at +25°C or 2 μA max over temperature, making the device suitable for use in portable battery powered equipment. The internal reference resistors, the reference bias servo loop, the output amplifier and associated linear circuitry are all shut down when the power-down is activated. The output terminal sees a load of ≈ 23 kΩ to GND when in power-down mode as shown in Figure 25. The contents of the data register are unaffected when in power-down mode. The device typically comes out of power-down in 13 μs (see Figure 10).

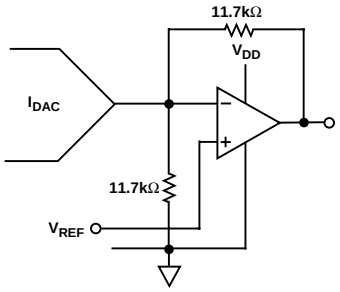


Figure 25. Output Stage During Power-Down

Analog Outputs

The AD7801 contains a voltage output DAC with 8-bit resolution and rail-to-rail operation. The output buffer provides a gain of two at the output. Figures 2, 3 and 4 show the source and sink capabilities of the output amplifier. The slew rate of the output amplifier is typically 7.5 V/μs and has a full-scale settling to eight bits with a 100 pF capacitive load in typically 1.2 μs.

The input coding to the DAC is straight binary. Table I shows the binary transfer function for the AD7801. Figure 26 shows the DAC transfer function for binary coding. Any DAC output voltage can be expressed as:

$$V_{OUT} = 2 \times V_{REF}\left(\frac{N}{256}\right)$$

where:

N is the decimal equivalent of the binary input code. N ranges from 0 to 255.

V_{REF} is the voltage applied to the external REFIN pin when the external reference is selected and is $V_{DD}/2$ if the internal reference is used.

Table I. Output Voltage for Selected Input Codes

Digital MSB . . . LSB	Analog Output
1111 1111	$2 \times \frac{255}{256} \times V_{REF} V$
1111 1110	$2 \times \frac{254}{256} \times V_{REF} V$
1000 0001	$2 \times \frac{129}{256} \times V_{REF} V$
1000 0000	V_{REF} V
0111 1111	$2 \times \frac{127}{256} \times V_{REF} V$
0000 0001	$2 \times \frac{V_{REF}}{256} V$
0000 0000	0 V

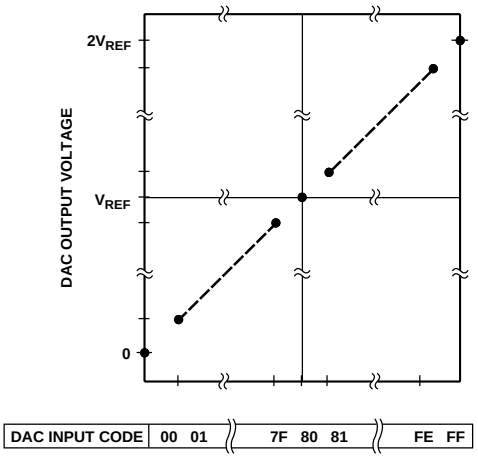


Figure 26. DAC Transfer Function

Figure 27 shows a typical setup for the AD7801 when using its internal reference. The internal reference is selected by tying the REFIN pin to V_{DD}. Internally in the reference section there is a reference detect circuit that will select the internal $V_{DD}/2$ based on the voltage connected to the REFIN pin. If REFIN is within a threshold voltage of a PMOS device (approximately 1 V) of V_{DD} the internal reference is selected. When the REFIN voltage is more than 1 V below V_{DD}, the externally applied voltage at this pin is used as the reference for the DAC. The internal reference on the AD7801 is $V_{DD}/2$, the output current to voltage converter within the AD7801 provides a gain of two. Thus the output range of the DAC is from 0 V to V_{DD}, based on Table I.

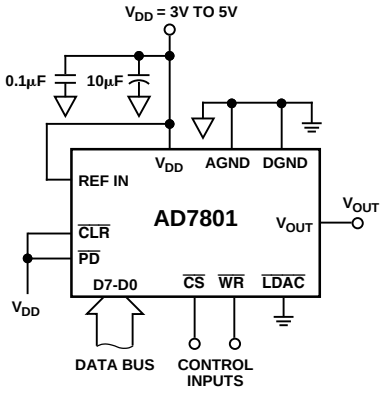


Figure 27. Typical Configuration Selecting the Internal Reference

Figure 28 shows a typical setup for the AD7801 when using an external reference. The reference range for the AD7801 is from 1 V to $V_{DD}/2$ V. Higher values of reference can be incorporated but will saturate the output at both the top and bottom end of the transfer function. There is a gain of two from input to output on the AD7801. Suitable references for 5 V operation are the AD780 and REF192. For 3 V operation a suitable external reference would be the AD589 a 1.23 V bandgap reference.

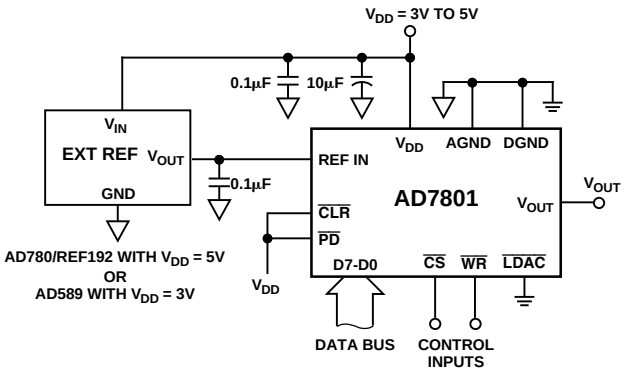


Figure 28. Typical Configuration Using An External Reference

MICROPROCESSOR INTERFACING

AD7801–ADSP-2101/ADSP-2103 Interface

Figure 29 shows an interface between the AD7801 and the ADSP-2101/ADSP-2103. The fast interface timing associated with the AD7801 allows easy interface to the ADSP-2101/ADSP-2103.

$\overline{\text{LDAC}}$ is permanently tied low in this circuit so the DAC output is updated on the rising edge of the $\overline{\text{WR}}$ signal.

Data is loaded to the AD7801 input register using the following ADSP-21xx instruction.

DM(DAC) = MR0

MR0 = ADSP-21xx MR0 Register.
DAC = Decoded DAC Address.

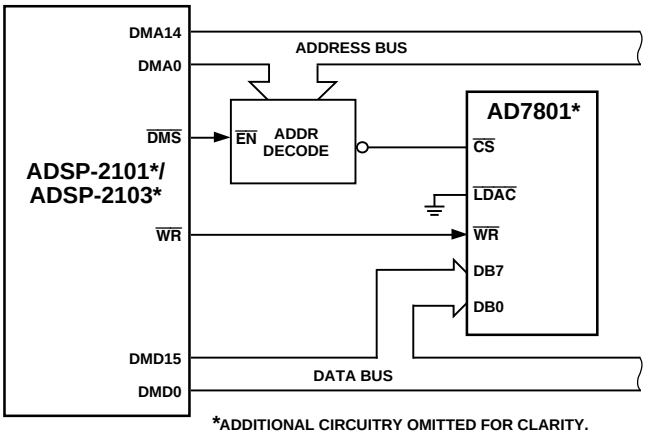


Figure 29. AD7801–ADSP-2101/ADSP-2103 Interface

AD7801–TMS320C20 Interface

Figure 30 shows an interface between the AD7801 and the TMS320C20. Data is loaded to the AD7801 using the following instruction:

OUT DAC, D

DAC = Decoded DAC Address.
D = Data Memory Address.

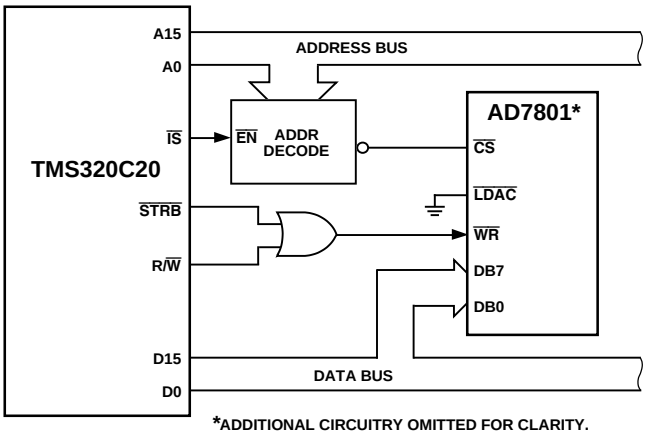


Figure 30. AD7801–TMS320C20 Interface

In the circuit shown the $\overline{LDAC}$ is hardwired low thus the DAC output is updated on the rising edge of $\overline{WR}$. Some applications may require synchronous updating of the DAC in the AD7801. In this case the $\overline{LDAC}$ signal can be driven from an external timer or can be controlled by the microprocessor. One option for synchronous updating is to decode the $\overline{LDAC}$ from the address bus so a write operation at this address will synchronously update the DAC output. A simple OR gate with one input driven from the decoded address and the second input from the $\overline{WR}$ signal will implement this function.

AD7801–8051/8088 Interface

Figure 31 shows a serial interface between the AD7801 and the 8051/8088 processors.

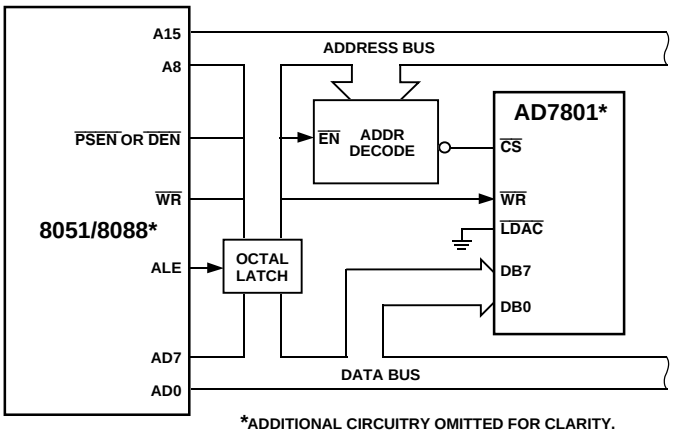


Figure 31. AD7801–8051/8088 Interface

APPLICATIONS

Bipolar Operation Using the AD7801

The AD7801 has been designed for unipolar operation but bipolar operation is possible using the circuit in Figure 32. The circuit shown is configured for an output voltage range of –5 V to +5 V. Rail-to-rail operation at the amplifier output is achievable by using an AD820 or OP295 as the output amplifier.

The output voltage for any input code can be calculated as follows:

$$V_O = \left[R_2\left(1+\frac{R4}{R3}\right)/\left(R1+R2\right)\times\left(\frac{2V_{REF}D}{256}\right)-V_{REF}\left(\frac{R4}{R3}\right)\right]$$

Where D is the decimal equivalent of the code loaded to the DAC and V_{REF} is the reference voltage input.

With V_{REF} = 2.5 V, R1 = R3 = 10 kΩ and R2 = R4 = 20 kΩ and V_{DD} = 5 V.

$$V_O = \left(\frac{10D}{256}\right)-5$$

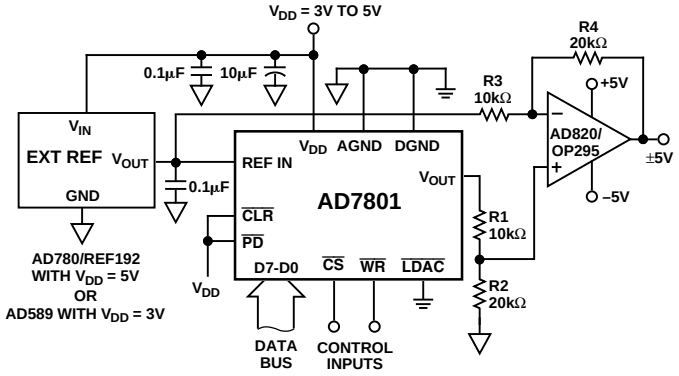


Figure 32. Bipolar Operation Using the AD7801

Decoding Multiple AD7801s in a System

The $\overline{CS}$ pin on the AD7801 can be used in applications to decode a number of DACs. In this application, all DACs in the system receive the same input data, but only the $\overline{CS}$ to one of the DACs will be active at any one time allowing access to one channel in the system. The 74HC139 is used as a two-to-four line decoder to address any of the DACs in the system. To prevent timing errors from occurring, the Enable input on the 74HC139 should be brought to its inactive state while the Coded Address inputs are changing state. Figure 33 shows a diagram of a typical setup for decoding multiple AD7801 devices in a system. The built-in power-on reset circuit on the AD7801 ensures that the outputs of all DACs in the system power up with zero volts on their outputs.

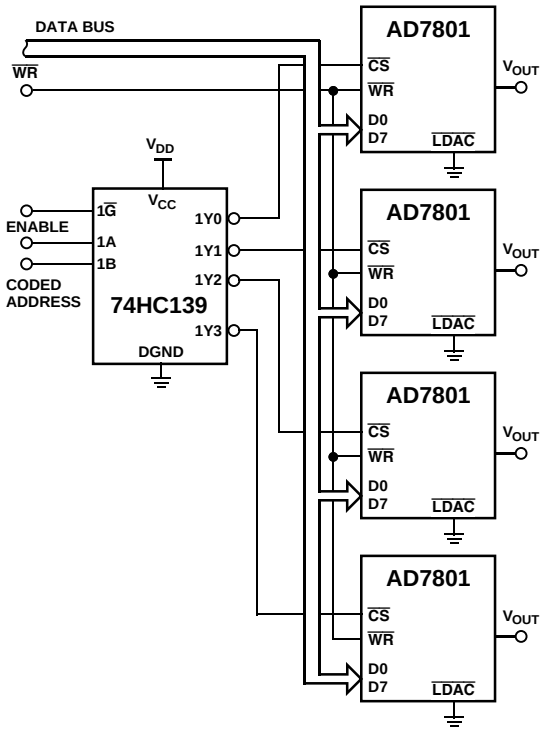


Figure 33. Decoding Multiple AD7801s

AD7801 as a Digitally Programmable Indicator

A digitally programmable upper limit detector using the DAC is shown in Figure 34. The upper limit for the test is loaded to the DAC, which in turn sets the limit for the CMP04. If a signal at the V_{IN} input is not below the programmed value, an LED will indicate the Fail condition.

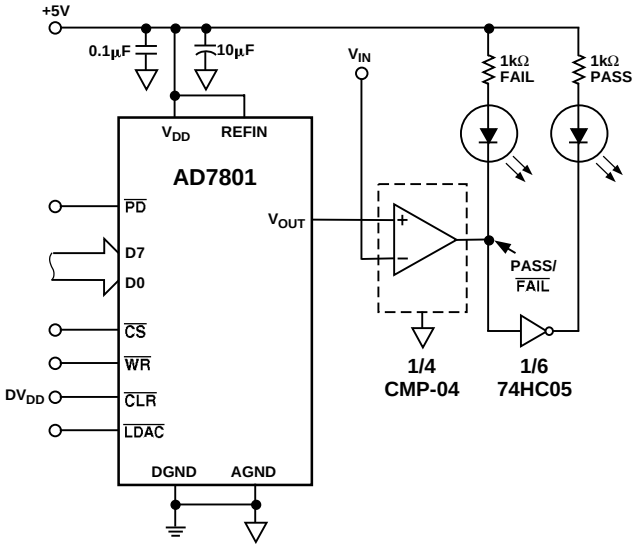


Figure 34. Digitally Programmable Indicator

Programmable Current Source

Figure 35 shows the AD7801 used as the control element of a programmable current source. In this circuit the full-scale current is set to 1 mA. The output voltage from the DAC is applied across the current setting resistor of 4.7 kΩ in series with the full-scale setting resistor of 470 Ω. Suitable transistors to place in the feedback loop of the amplifier include the BC107 and the 2N3904, which enable the current source to operate from a minimum V_{SOURCE} of 6 V. The operating range is determined by the operating characteristics of the transistor. Suitable amplifiers include the AD820 and the OP295, both of which have rail-to-rail operation on their outputs. The current for any digital input code can be calculated as follows:

$$I = \frac{\left(2\,V_{REF}\,D\right)}{\left(256\ (5\ k\Omega)\right)}$$

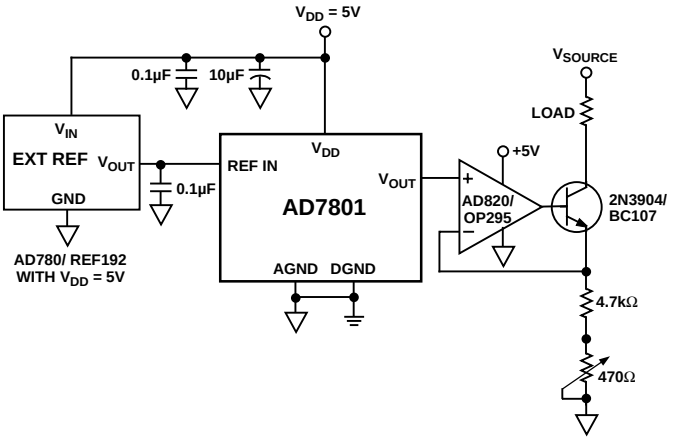


Figure 35. Programmable Current Source

Coarse and Fine Adjustment using two AD7801s

The two DACs can be paired together to form a coarse and fine adjustment function for a setpoint as shown in Figure 36. In this circuit, the first DAC is used to provide the coarse adjustment and the second DAC is used to provide the fine adjustment. Varying the ratio of R1 and R2 will vary the relative effect of the coarse and fine tune elements in the circuit. For the resistor values shown, the second DAC has a resolution of 148 µV giving a fine tune range of 38 mV (approximately 2 LSB) for operation with a V_{DD} of 5 V and a reference of 2.5 V. The amplifier shown allows a rail-to-rail output voltage to be achieved on the output. A typical application for the circuit would be in a setpoint controller.

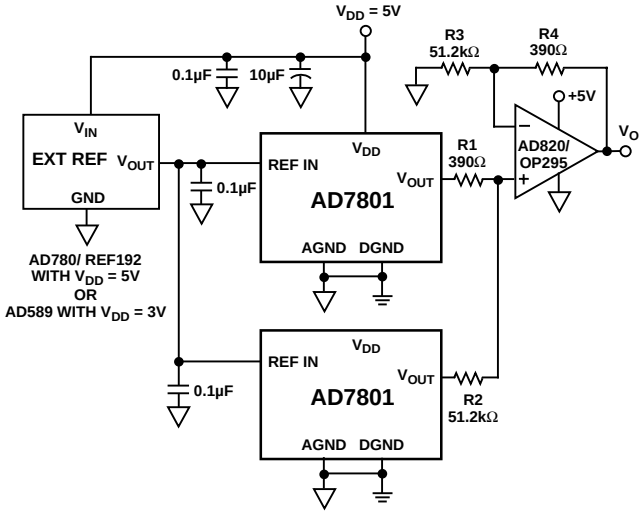


Figure 36. Coarse and Fine Adjustment

Power Supply Bypassing and Grounding

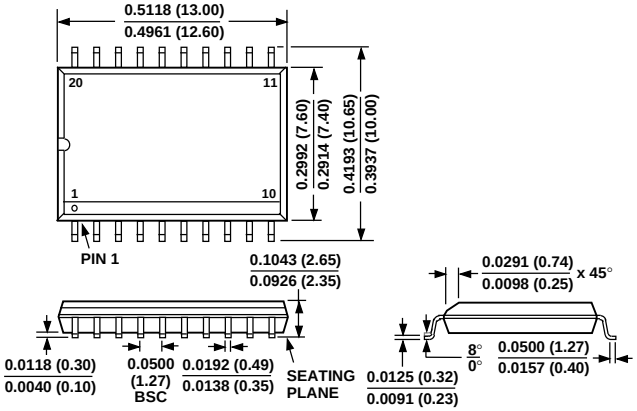
In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD7801 is mounted should be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the AD7801 is in a system where multiple devices require an AGND to DGND connection, the connection should be made at one point only, a star ground point which should be established as closely as possible to the AD7801. The AD7801 should have ample supply bypassing of 10 µF in parallel with 0.1 µF located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitors should have low Effective Series Resistance (ESR) and Effective Series Inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

The power supply lines of the AD7801 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the supply line. Fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other parts of the board and should never be run near reference inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effect of feedthrough through the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to the ground plane while signal traces are placed on the solder side.

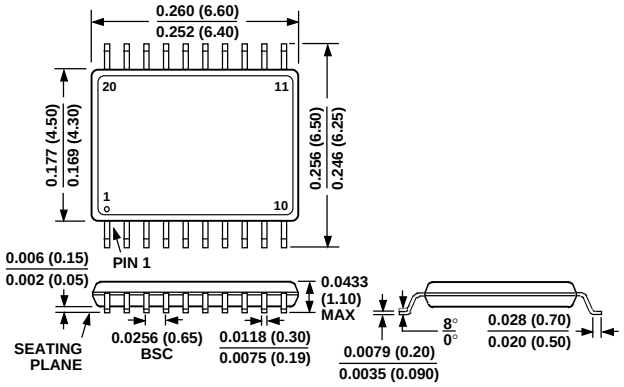
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

20-Lead Wide Body SOIC
(R-20)



20-Lead TSSOP
(RU-20)



C2995–12–4/97

PRINTED IN U.S.A.

ANALOG DEVICES

Very Low Noise Quad Operational Amplifier

OP-470

FEATURES

- **Very Low Noise** ..... **5nV/$\sqrt{Hz}$ @ 1kHz Max**
- **Excellent Input Offset Voltage** ..... **0.4mV Max**
- **Low Offset Voltage Drift** ..... **2μV/°C Max**
- **Very High Gain** ..... **1000V/mV Min**
- **Outstanding CMR** ..... **110dB Min**
- **Slew Rate** ..... **2V/μs Typ**
- **Gain-Bandwidth Product** ..... **6MHz Typ**
- **Industry Standard Quad Pinouts**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (μV)	PACKAGE			OPERATING TEMPERATURE RANGE
	CERDIP 14-PIN	PLASTIC	LCC*	
400	–	–	OP470ARC/883	MIL
400	OP470AY*	–	OP470ATC/883	MIL
400	OP470EY	–	–	IND
800	OP470FY	–	–	IND
1000	–	OP470GP	–	XIND
1000	–	OP470GS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

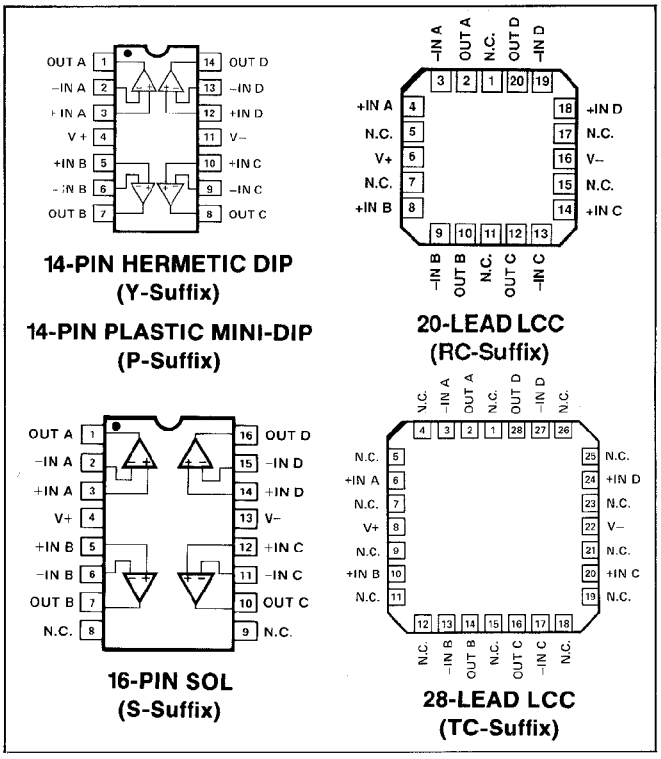
†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

The OP-470 is a high-performance monolithic quad operational amplifier with exceptionally low voltage noise, 5nV/$\sqrt{Hz}$ at 1kHz Max, offering comparable performance to PMI's industry standard OP-27.

The OP-470 features an input offset voltage below 0.4mV, excellent for a quad op amp, and an offset drift under 2μV/°C, guaranteed over the full military temperature range. Open-loop gain of the OP-470 is over 1,000,000 into a 10kΩ load insuring excellent gain accuracy and linearity, even in high-gain applications. Input bias current is under 25nA which reduces errors due to signal source resistance. The OP-470's CMR of over 110dB and PSRR of less than 1.8μV/V significantly reduce errors due to ground noise and power supply fluctuations. Power consumption of the quad OP-470 is half that of four OP-27s, a significant advantage for power con-

PIN CONNECTIONS



14-PIN HERMETIC DIP (Y-Suffix)

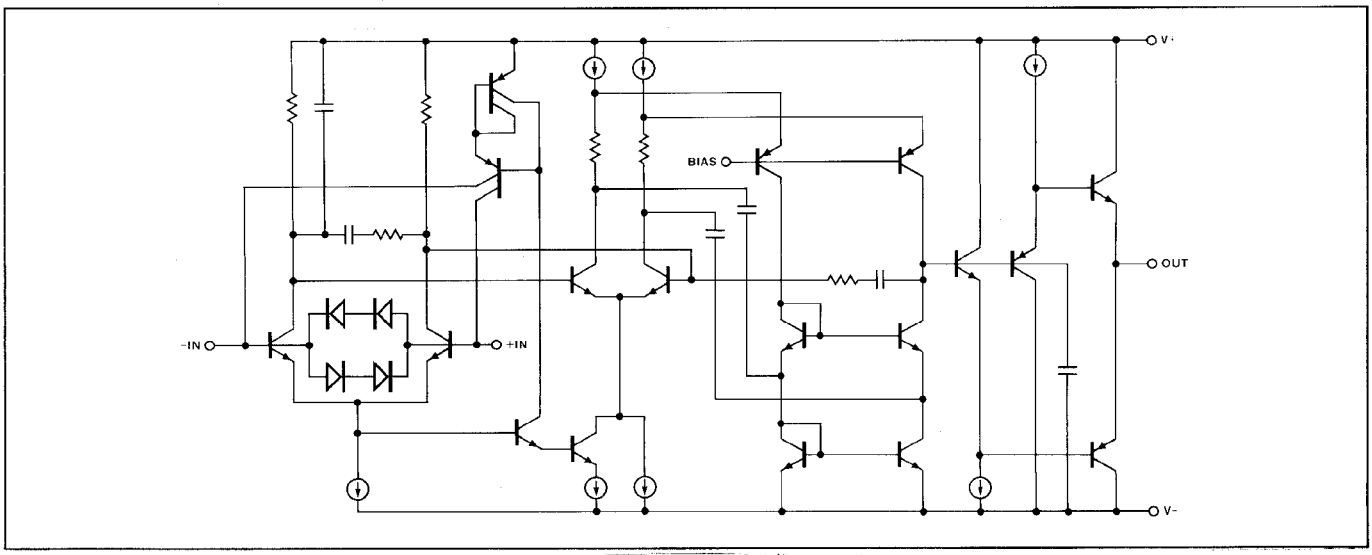
14-PIN PLASTIC MINI-DIP (P-Suffix)

20-LEAD LCC (RC-Suffix)

16-PIN SOL (S-Suffix)

28-LEAD LCC (TC-Suffix)

SIMPLIFIED SCHEMATIC



scious applications. The OP-470 is unity-gain stable with a gain-bandwidth product of 6MHz and a slew rate of 2V/μs.

The OP-470 offers excellent amplifier matching which is important for applications such as multiple gain blocks, low-noise instrumentation amplifiers, quad buffers, and low-noise active filters.

The OP-470 conforms to the industry standard 14-pin DIP pinout. It is pin compatible with the OP-11, LM148/149, HA4741, HA5104, and RM4156 quad op amps and can be used to upgrade systems using these devices.

For higher speed applications the OP-471, with a slew rate of 8V/μs, is recommended.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Differential Input Voltage (Note 2) ..... ±1.0V
Differential Input Current (Note 2) ..... ±25mA
Input Voltage ..... Supply Voltage
Output Short-Circuit Duration ..... Continuous
Storage Temperature Range
P, TC, Y-Package ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Junction Temperature (T_j) ..... –65°C to +150°C
Operating Temperature Range
OP-470A ..... –55°C to +125°C
OP-470E, OP-470F ..... –25°C to +85°C
OP-470G ..... –40°C to +85°C

PACKAGE TYPE	Θ_{jA} (Note 3)	Θ_{jC}	UNITS
14-Pin Hermetic DIP (Y)	94	10	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W
20-Contact LCC (RC)	78	30	°C/W
28-Contact LCC (TC)	70	28	°C/W
16-Pin SOL (S)	88	23	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. The OP-470's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise performance. If differential voltage exceeds ±1.0V, the input current should be limited to ±25mA.
3. Θ_{jA} is specified for worst case mounting conditions, i.e., Θ_{jA} is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages; Θ_{jA} is specified for device soldered to printed circuit board for SO and PLCC packages.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = 25°C, unless otherwise noted.

			OP-470A/E			OP-470F			OP-470G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.1	0.4	—	0.2	0.8	—	0.4	1.0	mV
Input Offset Current	I_{OS}	V_{CM} = 0V	—	3	10	—	6	20	—	12	30	nA
Input Bias Current	I_B	V_{CM} = 0V	—	6	25	—	15	50	—	25	60	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 1)	—	80	200	—	80	200	—	80	200	nV_{p-p}
Input Noise Voltage Density	e_n	f_O = 10Hz	—	3.8	6.5	—	3.8	6.5	—	3.8	6.5	$nV/\sqrt{Hz}$
		f_O = 100Hz	—	3.3	5.5	—	3.3	5.5	—	3.3	5.5	
		f_O = 1kHz (Note 2)	—	3.2	5.0	—	3.2	5.0	—	3.2	5.0	
Input Noise Current Density	i_n	f_O = 10Hz	—	1.7	—	—	1.7	—	—	1.7	—	$pA/\sqrt{Hz}$
		f_O = 100Hz	—	0.7	—	—	0.7	—	—	0.7	—	
		f_O = 1kHz	—	0.4	—	—	0.4	—	—	0.4	—	
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V										V/mV
		R_L = 10kΩ	1000	2300	—	800	1700	—	800	1700	—	
		R_L = 2kΩ	500	1200	—	400	900	—	400	900	—	
Input Voltage Range	IVR	(Note 3)	±11	±12	—	±11	±12	—	±11	±12	—	V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13	—	±12	±13	—	±12	±13	—	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	110	125	—	100	120	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	—	0.56	1.8	—	1.0	5.6	—	1.0	5.6	μV/V
Slew Rate	SR		1.4	2	—	1.4	2	—	1.4	2	—	V/μs

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-470A/E MIN	OP-470A/E TYP	OP-470A/E MAX	OP-470F MIN	OP-470F TYP	OP-470F MAX	OP-470G MIN	OP-470G TYP	OP-470G MAX	UNITS
Supply Current (All Amplifiers)	I_{SY}	No Load	—	9	11	—	9	11	—	9	11	mA
Gain Bandwidth Product	GBW	$A_V = +10$	—	6	—	—	6	—	—	6	—	MHz
Channel Separation	CS	$V_O = 20V_{p-p}$ $f_O = 10Hz$ (Note 1)	125	155	—	125	155	—	125	155	—	dB
Input Capacitance	C_{IN}		—	2	—	—	2	—	—	2	—	pF
Input Resistance Differential-Mode	R_{IN}		—	0.4	—	—	0.4	—	—	0.4	—	MΩ
Input Resistance Common-Mode	R_{INCM}		—	11	—	—	11	—	—	11	—	GΩ
Settling Time	t_s	$A_V = +1$ to 0.1% to 0.01%	— —	5.5 6.0	— —	— —	5.5 6.0	— —	— —	5.5 6.0	— —	μs

NOTES:
1. Guaranteed but not 100% tested.
2. Sample tested.
3. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55°C \leq T_A \leq 125°C$ for OP-470A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-470A MIN	OP-470A TYP	OP-470A MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.14	0.6	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.4	2	μV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	5	20	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	15	50	nA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	750 400	1600 800	— —	V/mV
Input Voltage Range	IVR	(Note 1)	±11	±12	—	V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±13	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	1.0	5.6	μV/V
Supply Current (All Amplifiers)	I_{SY}	No Load	—	9.2	11	mA

NOTE:
1. Guaranteed by CMR test.

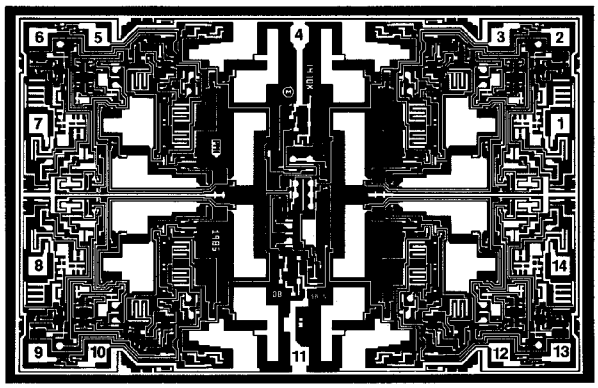
OP-470

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-25°C \le T_A \le +85°C$ for OP-470E/F, $-40°C \le T_A \le +85°C$ for OP-470G, unless otherwise noted.

			OP-470E			OP-470F			OP-470G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}		—	0.12	0.5	—	0.24	1.0	—	0.5	1.5	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.4	2	—	0.6	4	—	2	—	µV/°C
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	4	20	—	7	40	—	20	50	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	11	50	—	20	70	—	40	75	nA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$										
		$R_L = 10k\Omega$	800	1800	—	600	1400	—	600	1500	—	V/mV
		$R_L = 2k\Omega$	400	900	—	300	700	—	300	800	—	
Input Voltage Range	IVR	(Note 1)	±11	±12	—	±11	±12	—	±11	±12	—	V
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12	±13	—	±12	±13	—	±12	±13	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	100	120	—	90	115	—	90	110	—	dB
Power Supply Rejection Ratio	PSRR	V_S – ±4.5V to ⊥18V	—	0.7	5.6	—	1.8	10	—	1.8	10	µV/V
Supply Current (All Amplifiers)	I_{SY}	No Load	—	9.2	11	—	9.2	11	—	9.3	11	mA

NOTE:
1. Guaranteed by CMR test.

DICE CHARACTERISTICS



1. OUT A
2. −IN A
3. +IN A
4. V+
5. +IN B
6. −IN B
7. OUT B
8. OUT C
9. −IN C
10. +IN C
11. V−
12. +IN D
13. −IN D
14. OUT D

DIE SIZE 0.163 × 0.106 inch, 17,278 sq. mils
(4.14 × 2.69 mm, 11.14 sq. mm)

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-470GBC LIMIT	UNITS
Input Offset Voltage	V_{OS}		0.8	mV MAX
Input Offset Current	I_{OS}	$V_{CM} = 0V$	20	nA MAX
Input Bias Current	I_B	$V_{CM} = 0V$	50	nA MAX
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	 800 400	 V/mV MIN
Input Voltage Range	IVR	(Note 1)	±11	V MIN
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	V MIN
Common Mode Rejection	CMR	$V_{CM} = \pm 11V$	100	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	5.6	μV/V MAX
Slew Rate	SR		1.4	V/μs MIN
Supply Current (All Amplifiers)	I_{SY}	No Load	11	mA MAX

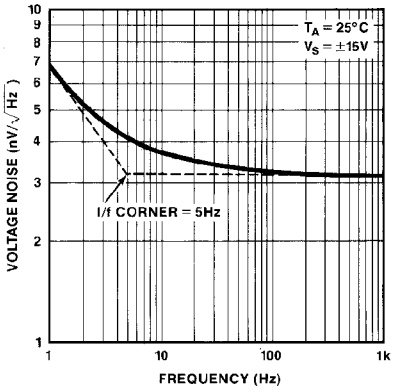
NOTE:
1. Guaranteed by CMR test.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

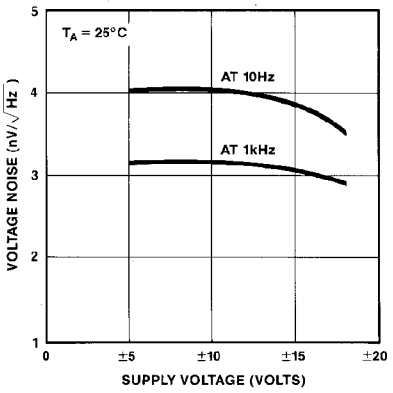
OP-470

TYPICAL PERFORMANCE CHARACTERISTICS

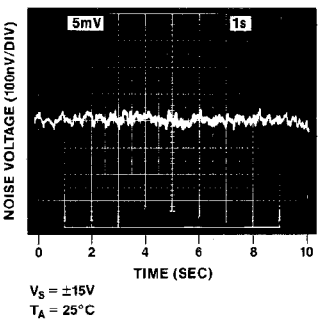
VOLTAGE NOISE DENSITY vs FREQUENCY



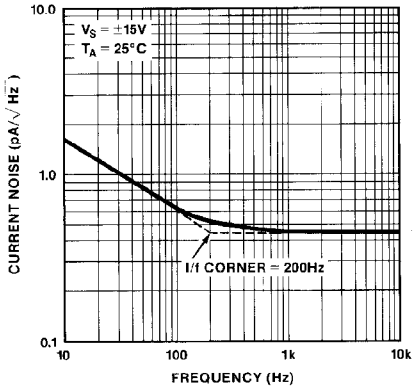
VOLTAGE NOISE DENSITY vs SUPPLY VOLTAGE



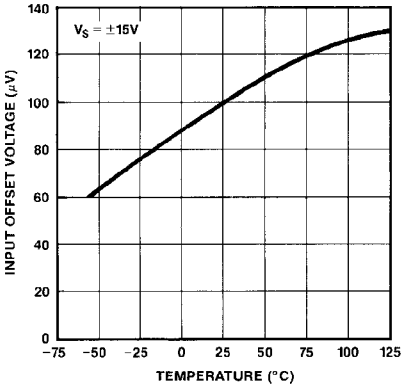
0.1Hz TO 10Hz NOISE



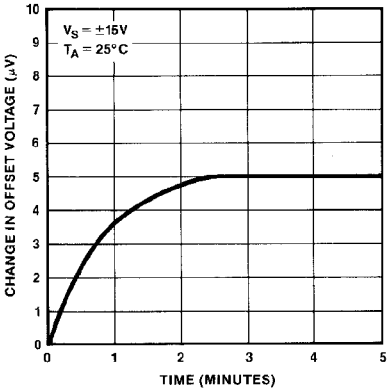
CURRENT NOISE DENSITY vs FREQUENCY



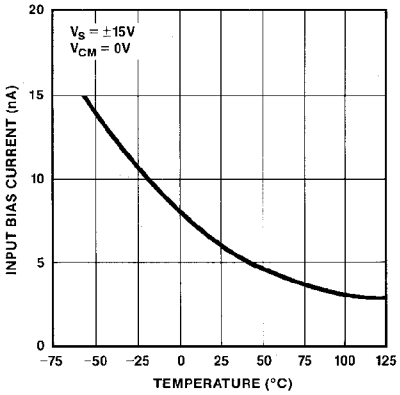
INPUT OFFSET VOLTAGE vs TEMPERATURE



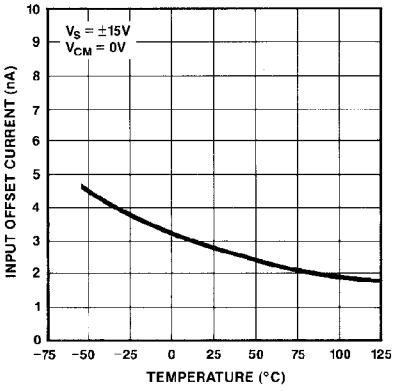
WARM-UP OFFSET VOLTAGE DRIFT



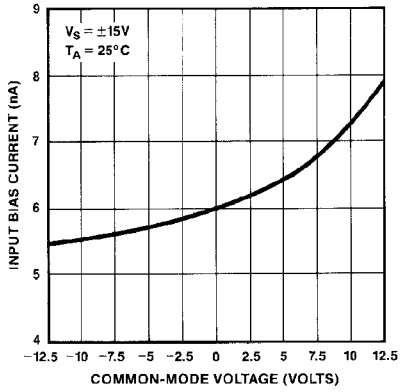
INPUT BIAS CURRENT vs TEMPERATURE



INPUT OFFSET CURRENT vs TEMPERATURE

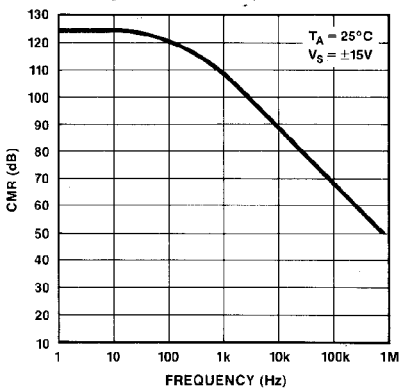


INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE

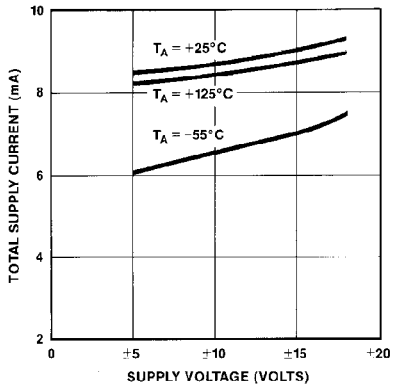


TYPICAL PERFORMANCE CHARACTERISTICS

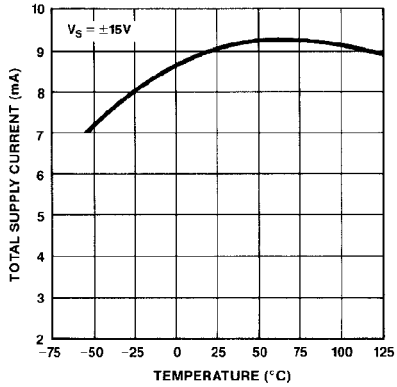
CMR vs FREQUENCY



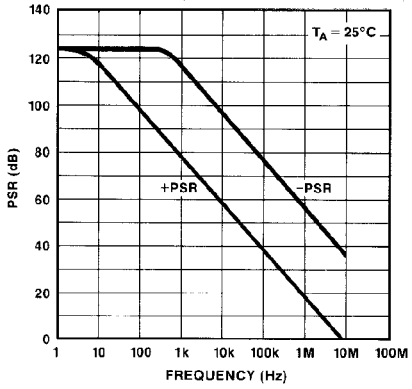
TOTAL SUPPLY CURRENT vs SUPPLY VOLTAGE



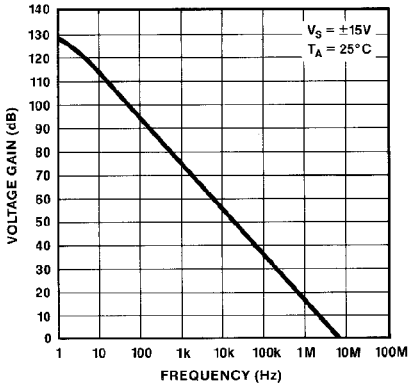
TOTAL SUPPLY CURRENT vs TEMPERATURE



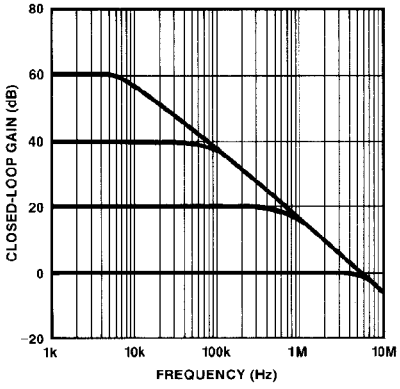
PSR vs FREQUENCY



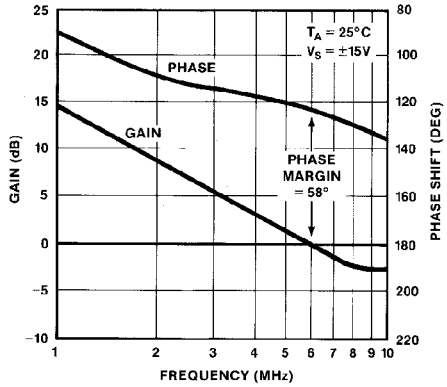
OPEN-LOOP GAIN vs FREQUENCY



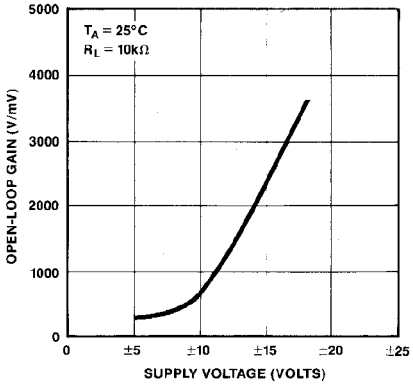
CLOSED-LOOP GAIN vs FREQUENCY



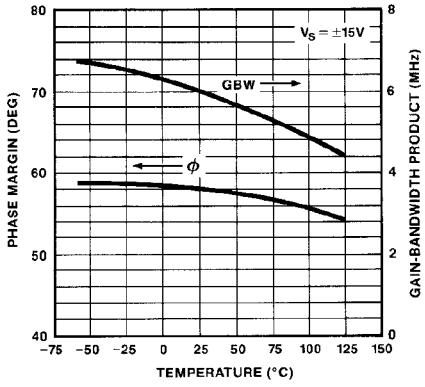
OPEN-LOOP GAIN, PHASE SHIFT vs FREQUENCY



OPEN-LOOP GAIN vs SUPPLY VOLTAGE



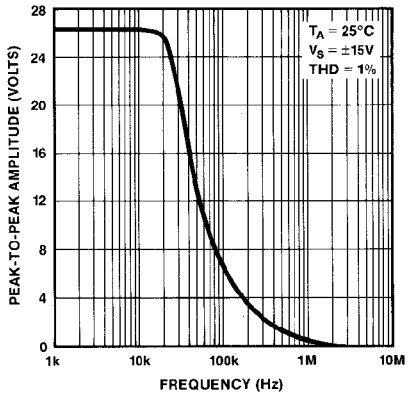
GAIN-BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE



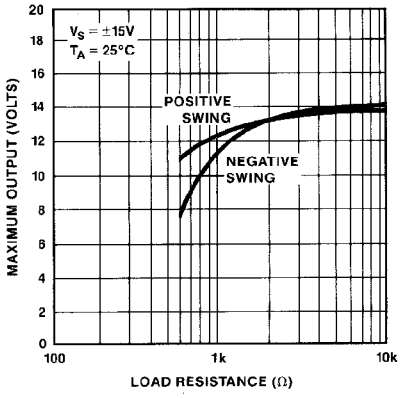
OP-470

TYPICAL PERFORMANCE CHARACTERISTICS

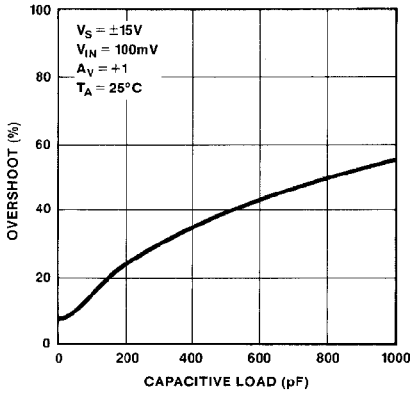
MAXIMUM OUTPUT SWING vs FREQUENCY



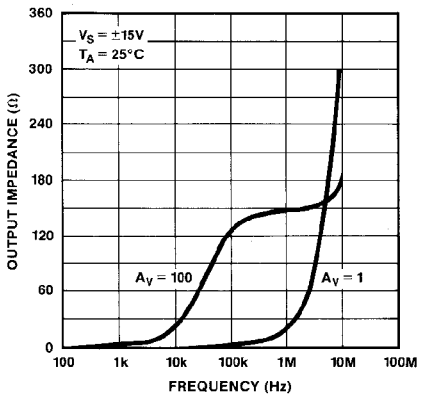
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



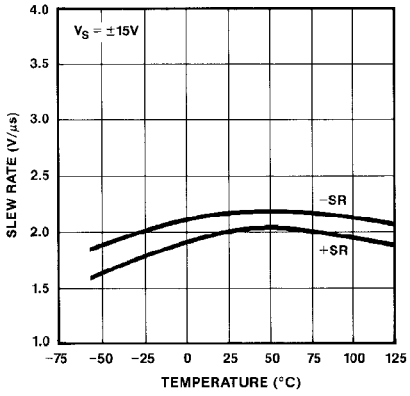
SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD



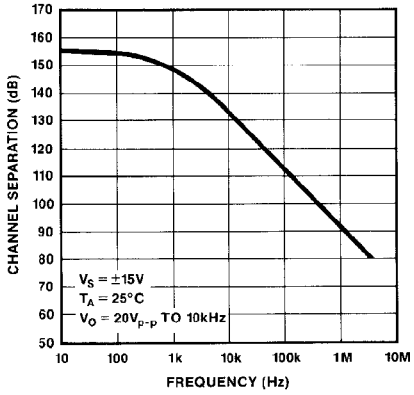
OUTPUT IMPEDANCE vs FREQUENCY



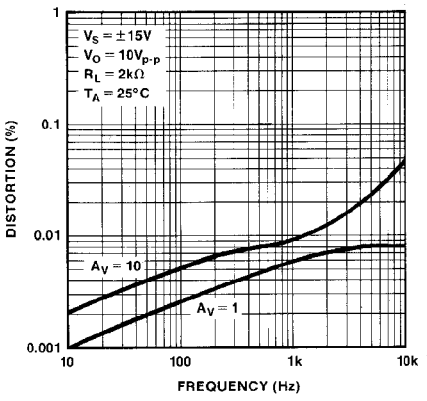
SLEW RATE vs TEMPERATURE



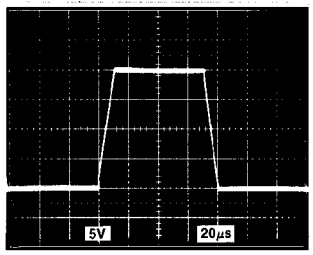
CHANNEL SEPARATION vs FREQUENCY



TOTAL HARMONIC DISTORTION vs FREQUENCY

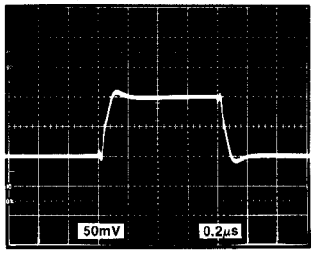


LARGE-SIGNAL TRANSIENT RESPONSE



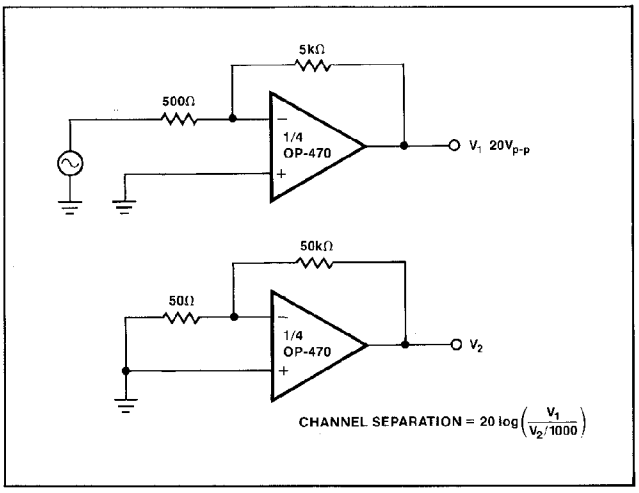
T_A = 25°C
V_S = ±15V
A_V = +1

SMALL-SIGNAL TRANSIENT RESPONSE

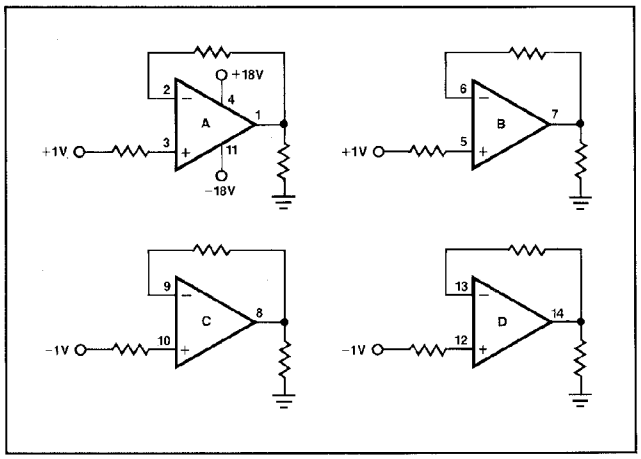


T_A = 25°C
V_S = ±15V
A_V = +1

CHANNEL SEPARATION TEST CIRCUIT



BURN-IN CIRCUIT



APPLICATIONS INFORMATION

VOLTAGE AND CURRENT NOISE

The OP-470 is a very low-noise quad op amp, exhibiting a typical voltage noise of only 3.2nV/$\sqrt{Hz}$ @ 1kHz. The exceptionally low noise characteristics of the OP-470 is in part achieved by operating the input transistors at high collector currents since the voltage noise is inversely proportional to the square root of the collector current. Current noise, however, is directly proportional to the square root of the collector current. As a result, the outstanding voltage noise performance of the OP-470 is gained at the expense of current noise performance, which is typical for low noise amplifiers.

To obtain the best noise performance in a circuit it is vital to understand the relationship between voltage noise (e_n), current noise (i_n), and resistor noise (e_t).

TOTAL NOISE AND SOURCE RESISTANCE

The total noise of an op amp can be calulated by:

$$E_n = \sqrt{(e_n)^2 + (i_n R_S)^2 + (e_t)^2}$$

where:

E_n = total input referred noise

e_n = op amp voltage noise

i_n = op amp current noise

e_t = source resistance thermal noise

R_S = source resistance

The total noise is referred to the input and at the output would be amplified by the circuit gain.

Figure 1 shows the relationship between total noise at 1kHz and source resistance. For $R_S < 1k\Omega$ the total noise is dominated by the voltage noise of the OP-470. As R_S rises above

FIGURE 1: Total Noise vs Source Resistance (Including Resistor Noise) at 1kHz

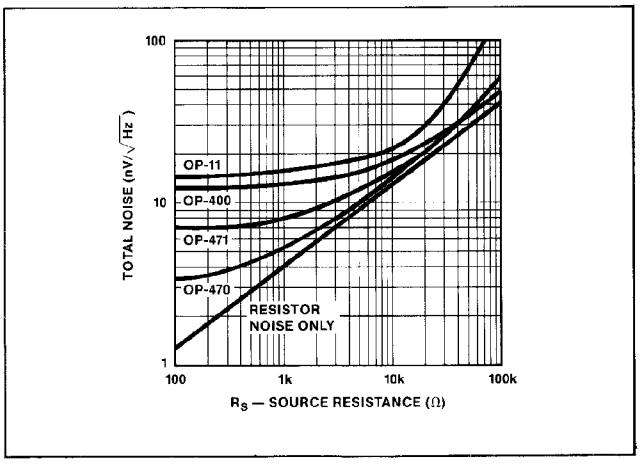
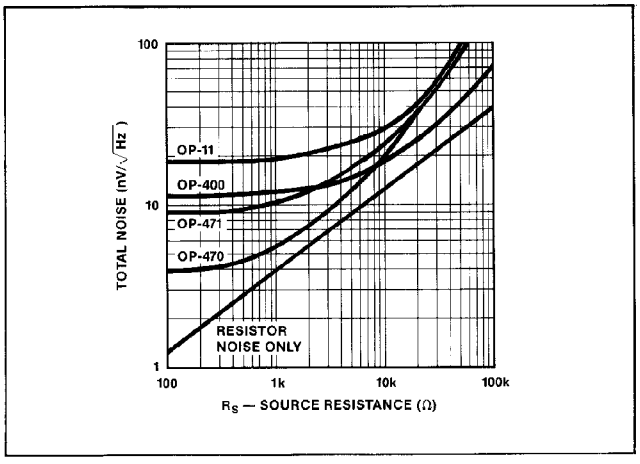


FIGURE 2: Total Noise vs Source Resistance (Including Resistor Noise) at 10Hz



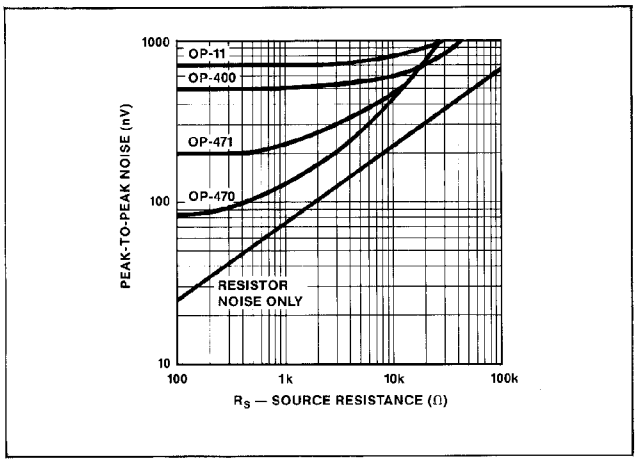
1kΩ, total noise increases and is dominated by resistor noise rather than by voltage or current noise of the OP-470. When R_S exceeds 20kΩ, current noise of the OP-470 becomes the major contributor to total noise.

Figure 2 also shows the relationship between total noise and source resistance, but at 10Hz. Total noise increases more quickly than shown in Figure 1 because current noise is inversely proportional to the square root of frequency. In Figure 2, current noise of the OP-470 dominates the total noise when $R_S > 5k\Omega$.

From Figures 1 and 2 it can be seen that to reduce total noise, source resistance must be kept to a minimum. In applications with a high source resistance, the OP-400, with lower current noise than the OP-470, will provide lower total noise.

Figure 3 shows peak-to-peak noise versus source resistance over the 0.1Hz to 10Hz range. Once again, at low values of R_S, the voltage noise of the OP-470 is the major contributor to peak-to-peak noise with current noise the major contributor as R_S increases. The crossover point between the OP-470 and the OP-400 for peak-to-peak noise is at $R_S = 17k\Omega$.

FIGURE 3: Peak-To-Peak Noise (0.1Hz To 10Hz) vs Source Resistance (Includes Resistor Noise)



The OP-471 is a higher speed version of the OP-470, with a slew rate of 8V/μs. Noise of the OP-471 is only slightly higher than the OP-470. Like the OP-470, the OP-471 is unity-gain stable.

For reference, typical source resistances of some signal sources are listed in Table I.

TABLE I

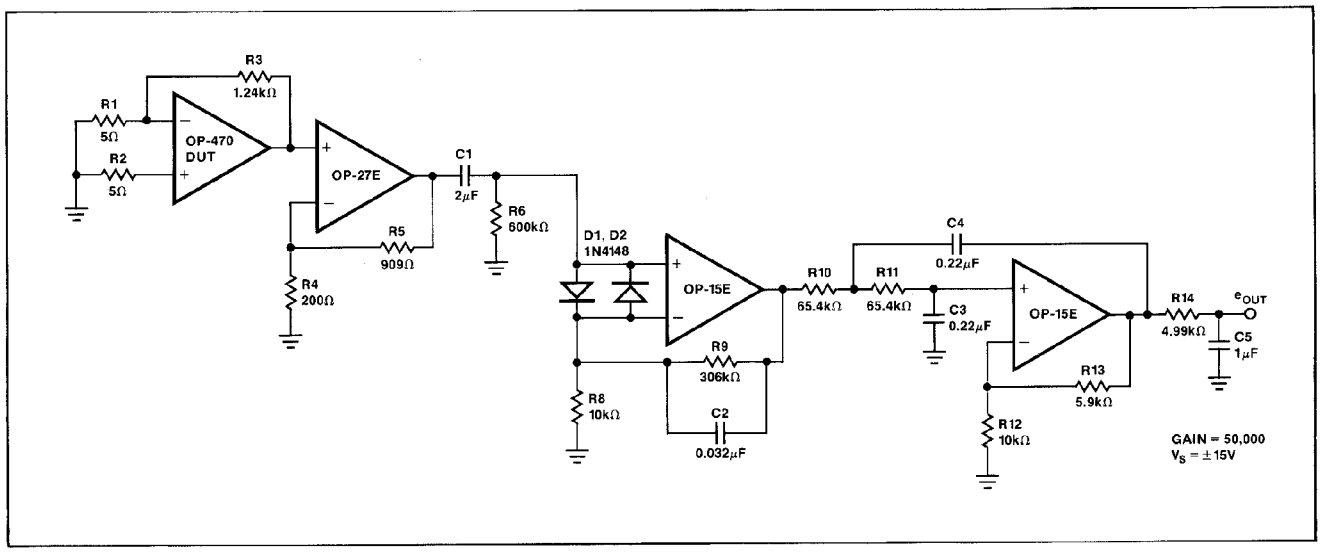
DEVICE	SOURCE IMPEDANCE	COMMENTS
Strain gauge	<500Ω	Typically used in low-frequency applications.
Magnetic tapehead	<1500Ω	Low I_B very important to reduce self-magnetization problems when direct coupling is used. OP-470 I_B can be neglected.
Magnetic phonograph cartridges	<1500Ω	Similar need for low I_B in direct coupled applications. OP-470 will not introduce any self-magnetization problem.
Linear variable differential transformer	<1500Ω	Used in rugged servo-feedback applications. Bandwidth of interest is 400Hz to 5kHz.

For further information regarding noise calculations, see "Minimization of Noise in Op-Amp Applications," Application Note AN-15.

NOISE MEASUREMENTS — PEAK-TO-PEAK VOLTAGE NOISE

The circuit of Figure 4 is a test setup for measuring peak-to-peak voltage noise. To measure the 200nV peak-to-peak

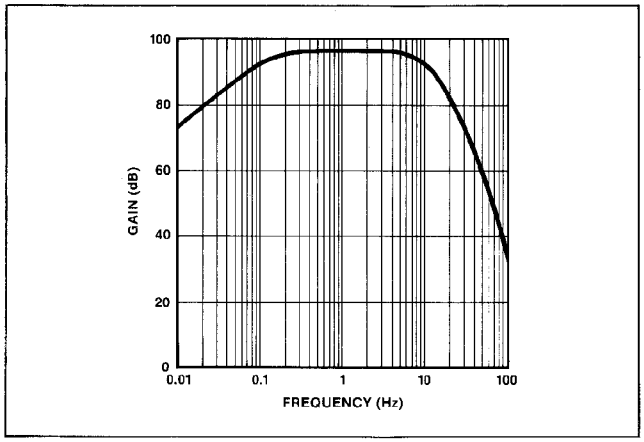
FIGURE 4: Peak-To-Peak Voltage Noise Test Circuit (0.1Hz To 10Hz)



noise specification of the OP-470 in the 0.1Hz to 10Hz range, the following precautions must be observed:

1. The device has to be warmed-up for at least five minutes. As shown in the warm-up drift curve, the offset voltage typically changes 5μV due to increasing chip temperature after power-up. In the 10-second measurement interval, these temperature-induced effects can exceed tens-of-nanovolts.
2. For similar reasons, the device has to be well-shielded from air currents. Shielding also minimizes thermocouple effects.
3. Sudden motion in the vicinity of the device can also "feed-through" to increase the observed noise.
4. The test time to measure 0.1Hz-to-10Hz noise should not exceed 10 seconds. As shown in the noise-tester frequency-response curve of Figure 5, the 0.1Hz corner is defined by only one pole. The test time of 10 seconds acts as an additional pole to eliminate noise contribution from the frequency band below 0.1Hz.
5. A noise-voltage-density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage-density measurement will correlate well with a 0.1Hz-to-10Hz peak-to-peak noise reading, since both results are determined by the white noise and the location of the 1/f corner frequency.
6. Power should be supplied to the test circuit by well bypassed low-noise supplies, e.g. batteries. These will minimize output noise introduced via the amplifier supply pins.

FIGURE 5: 0.1Hz To 10Hz Peak-To-Peak Voltage Noise Test Circuit Frequency Response



NOISE MEASUREMENT — NOISE VOLTAGE DENSITY

The circuit of Figure 6 shows a quick and reliable method of measuring the noise voltage density of quad op amps. Each individual amplifier is series-connected and is in unity-gain, save the final amplifier which is in a noninverting gain of 101. Since the ac noise voltages of each amplifier are uncorrelated, they add in rms fashion to yield:

$$e_{OUT} = 101\left(\sqrt{e_{nA}^2 + e_{nB}^2 + e_{nC}^2 + e_{nD}^2}\right)$$

The OP-470 is a monolithic device with four identical amplifiers. The noise voltage density of each individual amplifier will match, giving:

$$e_{OUT} = 101\left(\sqrt{4e_n^2}\right) = 101\ (2e_n)$$

FIGURE 6: Noise Voltage Density Test Circuit

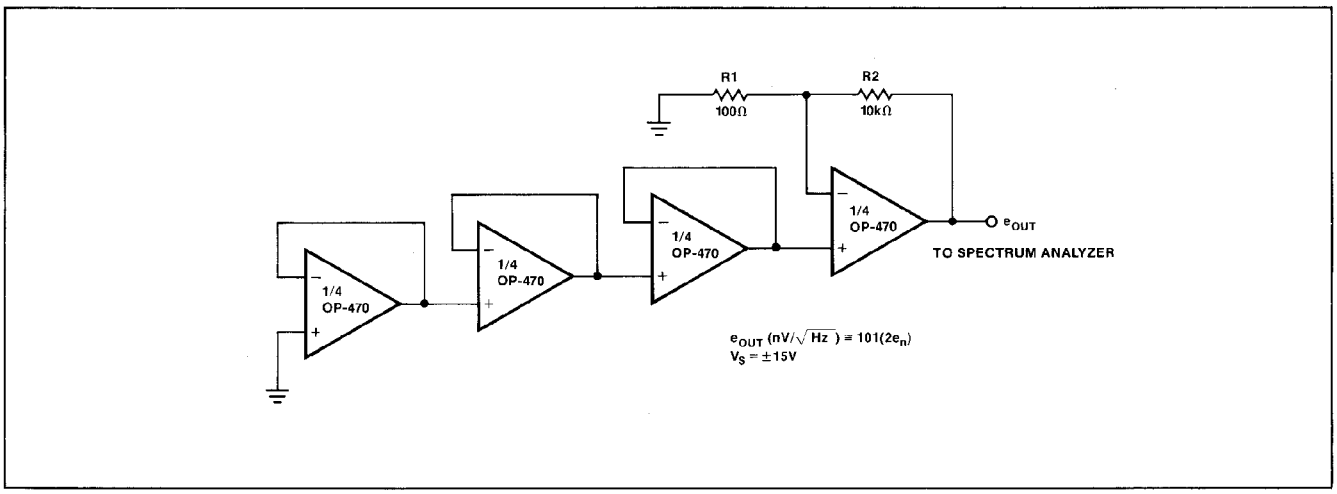
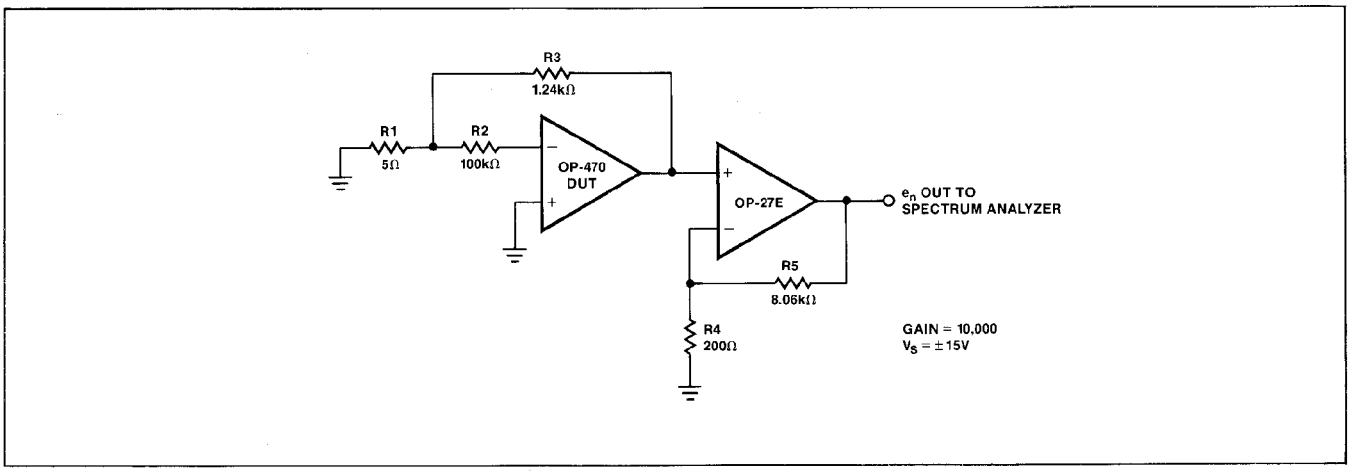


FIGURE 7: Current Noise Density Test Circuit



NOISE MEASUREMENT — CURRENT NOISE DENSITY

The test circuit shown in Figure 7 can be used to measure current noise density. The formula relating the voltage output to current noise density is:

$$i_n = \frac{\sqrt{\left(\frac{e_{nOUT}}{G}\right)^2 - \left(40nV/\sqrt{Hz}\right)^2}}{R_S}$$

where:

G = gain of 10000
R_S = 100kΩ source resistance

CAPACITIVE LOAD DRIVING AND POWER SUPPLY CONSIDERATIONS

The OP-470 is unity-gain stable and is capable of driving large capacitive loads without oscillating. Nonetheless, good supply bypassing is highly recommended. Proper supply bypassing reduces problems caused by supply line noise and improves the capacitive load driving capability of the OP-470.

In the standard feedback amplifier, the op amp's output resistance combines with the load capacitance to form a low-pass filter that adds phase shift in the feedback network and reduces stability. A simple circuit to eliminate this effect is shown in Figure 8. The added components, C1 and R3, decouple the amplifier from the load capacitance and provide additional stability. The values of C1 and R3 shown in Figure 8 are for a load capacitance of up to 1000pF when used with the OP-470.

In applications where the OP-470's inverting or noninverting inputs are driven by a low source impedance (under 100Ω) or connected to ground, if V+ is applied before V−, or when V− is disconnected, excessive parasitic currents will flow. Most

FIGURE 8: Driving Large Capacitive Loads

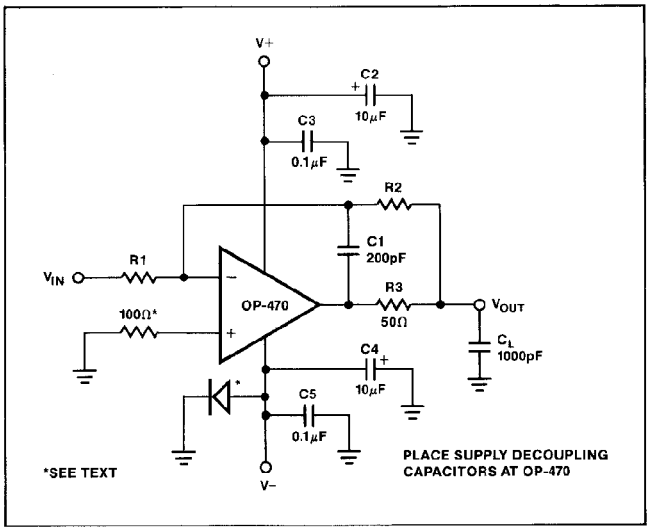
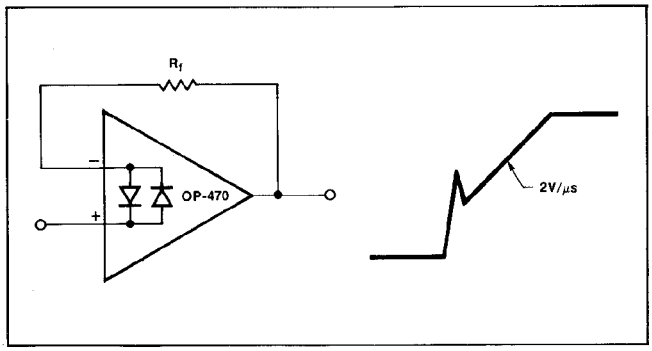


FIGURE 9: Pulsed Operation



applications use dual tracking supplies and with the device supply pins properly bypassed, power-up will not present a problem. A source resistance of at least 100Ω in series with all inputs (Figure 8) will limit the parasitic currents to a safe level if V– is disconnected. It should be noted that any source resistance, even 100Ω, adds noise to the circuit. Where noise is required to be kept at a minimum, a germanium or Schottky diode can be used to clamp the V– pin and eliminate the parasitic current flow instead of using series limiting resistors. For most applications, only one diode clamp is required per board or system.

UNITY-GAIN BUFFER APPLICATIONS

When $R_f \leq 100\Omega$ and the input is driven with a fast, large-signal pulse (>1V), the output waveform will look as shown in Figure 9.

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input, and a current, limited only by the output short-circuit protection, will be drawn by the signal generator. With $R_f \geq 500\Omega$, the output is capable of handling the current requirements ($I_L \leq 20mA$ at 10V); the amplifier will stay in its active mode and a smooth transition will occur.

When $R_f > 3k\Omega$, a pole created by R_f and the amplifier's input capacitance (2pF) creates additional phase shift and reduces phase margin. A small capacitor (20 to 50pF) in parallel with R_f helps eliminate this problem.

APPLICATIONS

LOW NOISE AMPLIFIER

A simple method of reducing amplifier noise by paralleling amplifiers is shown in Figure 10. Amplifier noise, depicted in Figure 11, is around $2nV/\sqrt{Hz}$ @ 1kHz (R.T.I.). Gain for each paralleled amplifier and the entire circuit is 1000. The 200Ω resistors limit circulating currents and provide an effective output resistance of 50Ω. The amplifier is stable with a 10nF capacitive load and can supply up to 30mA of output drive.

DIGITAL PANNING CONTROL

Figure 12 uses a DAC-8408, a quad 8-bit DAC, to pan a signal between two channels. The complementary DAC current outputs of two of the DAC-8408's four DACs drive current-to-voltage converters built from a single quad OP-470. The amplifiers have complementary outputs with the amplitudes dependent upon the digital code applied to the DAC. Figure 13 shows the complementary outputs for a 1kHz input signal and digital ramp applied to the DAC data inputs. Distortion of the digital panning control is less than 0.01%.

Gain error due to the mismatching between the internal DAC ladder resistors and the current-to-voltage feedback resistors is eliminated by using feedback resistors internal to the DAC. Of the four DACs available in the DAC-8408, only two, DACs A and C, actually pass a signal. DACs B and D are used to provide the additional feedback resistors needed in the circuit. If the $V_{REF}B$ and $V_{REF}D$ inputs remain unconnected the currrent-to-voltage converters using $R_{FB}B$ and $R_{FB}D$ are unaffected by digital data reaching DACs B and D.

FIGURE 10: Low Noise Amplifier

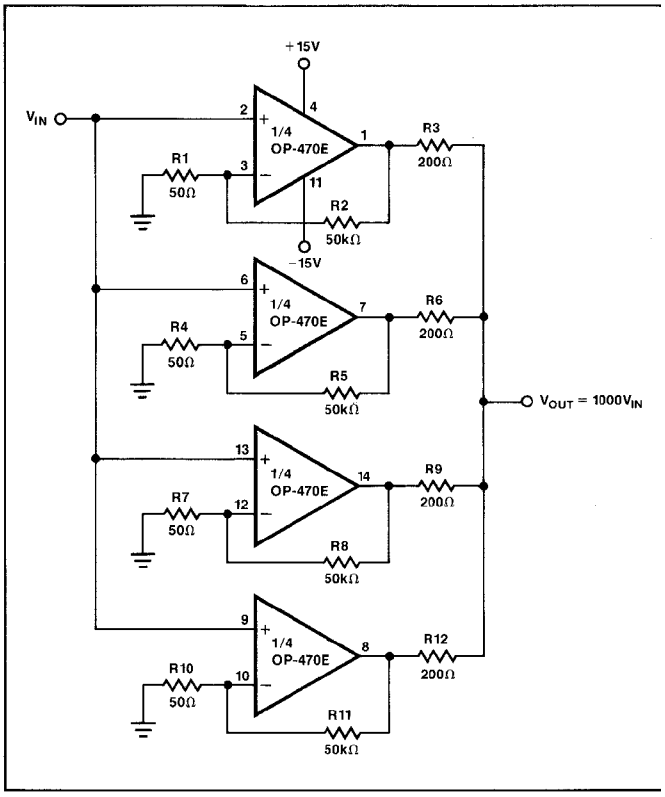


FIGURE 11: Noise Density of Low Noise Amplifier, G = 1000

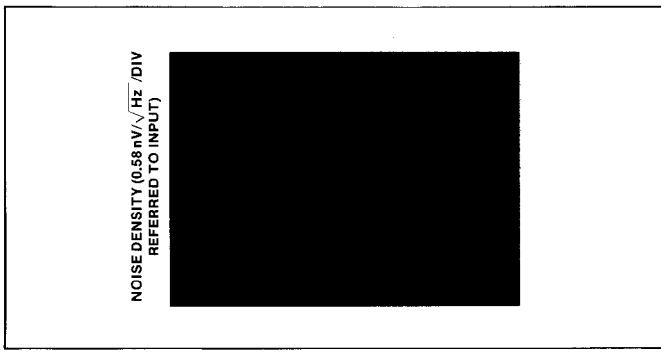


FIGURE 12: Digital Panning Control Circuit

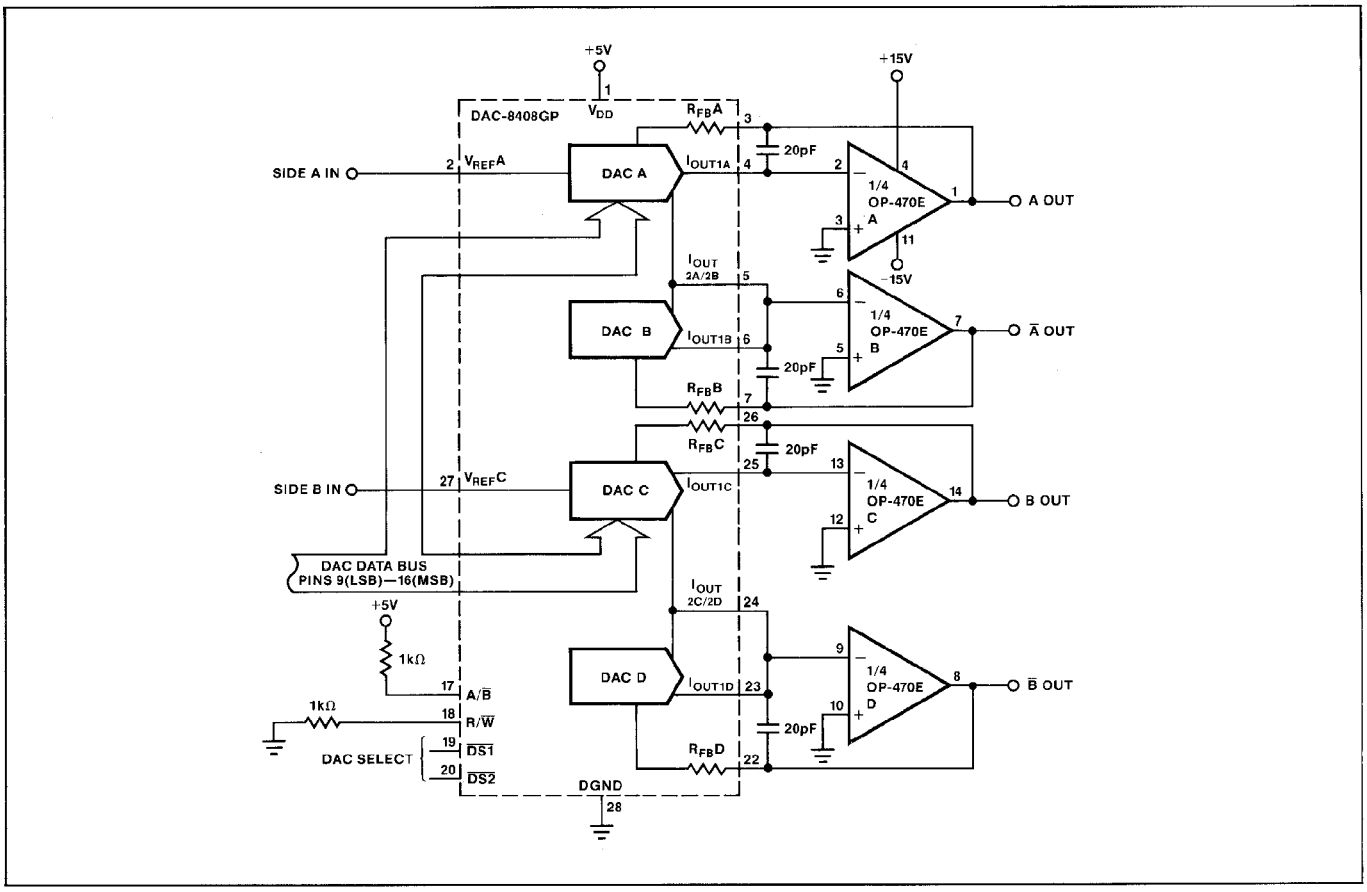


FIGURE 13: Digital Panning Control Output

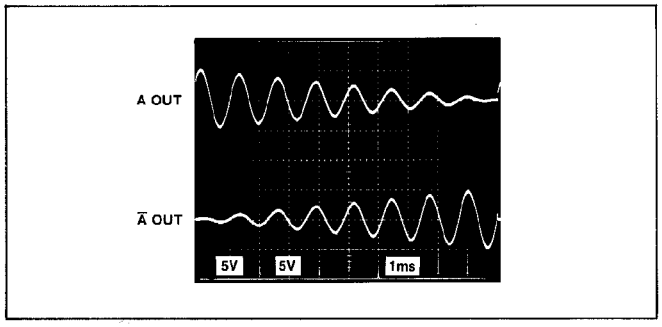
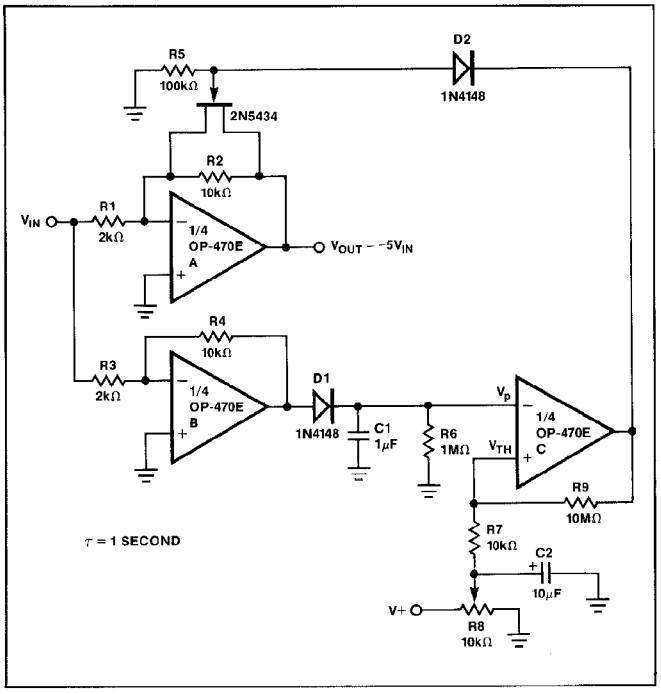


FIGURE 14: Squelch Amplifier



SQUELCH AMPLIFIER

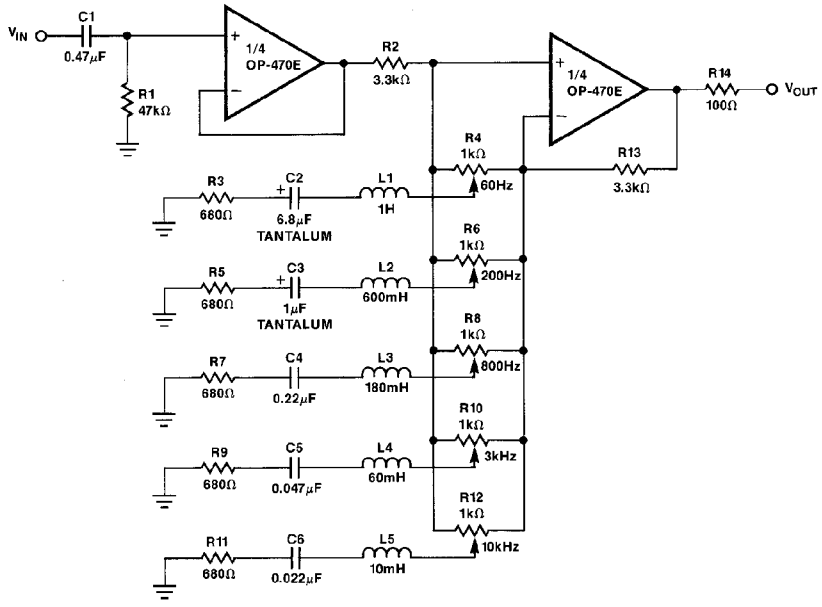
The circuit of Figure 14 is a simple squelch amplifier that uses a FET switch to cut off the output when the input signal falls below a preset limit.

The input signal is sampled by a peak detector with a time constant set by C1 and R6. When the output of the peak detector, V_p, falls below the threshold voltage, V_{TH}, set by R8, the comparator formed by op amp C switches from V− to V+. This drives the gate of the N-channel FET high, turning it ON, reducing the gain of the inverting amplifier formed by op amp A to zero.

FIVE-BAND LOW NOISE STEREO GRAPHIC EQUALIZER

The graphic equalizer circuit shown in Figure 15 provides 15dB of boost or cut over a 5-band range. Signal-to-noise ratio over a 20kHz bandwidth is better than 100dB referred to a 3V rms input. Larger inductors can be replaced by active inductors but this reduces the signal-to-noise ratio.

FIGURE 15: 5-Band Low Noise Graphic Equalizer



FREQUENCY MIXERS

Surface Mount

LEVEL 13 150 kHz to 6 GHz


ADE


ALY


† JMS


† LRMS-J

BLUE CELL™


MBA


MCA1

+13 dBm LO, up to +9 dBm RF

◆ MODEL NO.	FREQUENCY MHz LO/RF f_L-f_U	IF	CONVERSION LOSS dB Mid-Band $\bar{x}$	σ	Max.	Total Range Max.	LO-RF ISOLATION dB L Typ.	L Min.	M Typ.	M Min.	U Typ.	U Min.	LO-IF ISOLATION dB L Typ.	L Min.	M Typ.	M Min.	U Typ.	U Min.	IP3@ center band Typ. (dBm)	E factor	CASE STYLE	CONNECTION	PCB Lay-out PL-	PRICE $ Qty. (10-49)
◆ ADE-1MH**	2-500	DC-500	5.2	.10	6.5	8.0	60	45	50	35	48	25	55	40	45	30	40	22	17	0.4	CD542	ht	052	5.95
◆ ADE-1MHW**	0.5-600	DC-600	5.2	.10	6.9	8.0	63	50	53	32	43	20	56	40	44	25	30	20	17	0.4	CD636	ht	052	6.45
◆ ADE-10MH**	800-1000	10-200	7.0	0.2	—	8.5			34 (Typ.)		20 (Min.)				29 (Typ.)		20 (Min.)		26	1.3	CD636	ht	052	6.95
◆ ADE-12MH**	10-1200	DC-1200	6.3	.10	8.0	8.5	62	45	45	32	40	26	68	40	42	27	30	20	22	0.9	CD542	ht	052	6.45
◆ ADE-25MH**	5-2500	5-1500	6.9	.10	8.5	9.8	47	28	34	23	34	23	34	23	32	20	23	17	18	0.5	CD542	ht	052	6.95
◆ ADE-35MH**	5-3500	5-2500	6.9	.10	9.3	10.5	47	28	33	23	38	18	34	23	28	18	23	17	18	0.5	CD542	ht	052	9.95
◆ ADE-42MH**	5-4200	5-3500	7.5	.20	9.8	11.8	47	28	29	20	30	15	34	23	26	17	23	17	17	0.4	CD542	ht	052	14.95
◆ MBA-15MH*	1400-2400	DC-600	5.5	0.1	—	8.5			28 (Typ.)		16 (Min.)				16 (Typ.)		8 (Min.)		18	0.5	SM2	ld	066	7.95
◆ MBA-25MH*	2000-3000	DC-500	6.5	0.1	—	8.6			36 (Typ.)		18 (Min.)				20 (Typ.)		7 (Min.)		16	0.3	SM2	ld	066	7.95
NEW MCA1-24MH*	300-2400	DC-700	6.1	0.1	8.9				40		20				25		14		13	0	DZ885	ld	045	6.95
NEW MCA1-42MH*	1000-4200	DC-1500	6.2	0.1	8.9				32		20				20		10		16	0.3	DZ885	ld	045	7.95
NEW MCA1-60MH*	1600-4400	DC-2000	6.9	0.1	8.5				32		25				17		—		15	0.2	DZ885	ld	045	8.95
	4400-6000	DC-2000	6.0	0.1	8.5				22		18				15		—		15	0.2				
◆ ALY-44MH	2400-4400	DC-1400	7.5	.20	—	8.9			30 (Typ.)		20 (Min.)				20 (Typ.)		10 (Min.)		—		CB518	jy	085	18.95
◆ ALY-44MHW	1800-4900	DC-1400	7.5	.20	—	9.2			30 (Typ.)		20 (Min.)				14 (Typ.)		8 (Min.)		—		CB518	jy	085	19.95
JMS-1MH	2-500	DC-500	5.75	.10	7.0	8.0	70	55	60	40	44	25	55	42	45	25	35	20	—		BH292	ht	052	9.45
JMS-2MH	20-1000	DC-1000	7.0	.15	8.4	9.5	63	40	50	28	35	20	56	30	47	22	37	20	—		BH292	ht	052	10.45
JMS-5MH	5-1500	DC-1000	5.7	.10	8.0	9.5	67	40	57	25	35	20	60	40	35	18	15	8	—		BH292	ht	052	11.95
◆ LRMS-1MHJ	2-500	DC-500	5.65	.08	7.0	8.0	58	45	44	25	30	20	55	40	36	25	28	17	—		QQQ569	w	083	8.95
◆ LRMS-2MHJ	5-1000	DC-1000	6.72	.08	8.5	9.5	55	40	39	20	22	16	52	35	30	17	18	12	—		QQQ569	w	083	9.95
◆ LRMS-2UMHJ	10-1000	20-500	7.0	.10	8.5	9.5	52	40	43	30	33	25	53	30	44	25	39	22	—		QQQ569	w	083	14.45
◆ LRMS-5MHJ	10-1500	DC-900	5.67	.09	9.0	9.5	58	40	40	20	26	18	50	30	38	18	17	8	—		QQQ569	w	083	15.95

E= [IP3(dBm)-LO Power(dBm)]/10

L = low range [f_L to 10 f_L] M = mid range [10 f_L to f_U/2] U = upper range [f_U/2 to f_U]
m = mid band [2f_L to f_U/2]

NOTES:

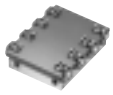
$\bar{x}$ Average of conversion loss at center of mid-band frequency (f_L+f_U/4)
σ Standard deviation
◆ Aqueous washable. For non-aqueous requirements, LRMS units available in case style QQQ130.
❑ Non-hermetic
† Phase detection, positive polarity
‡ Conversion loss increases up to 6 dB higher as IF frequency decreases from 5 MHz to DC.
✪ Frequency Specified RMS-42MH m=1000 - 2000 MHz, L=800 - 2100 MHz, U=2100 - 4200 MHz; TUF-2MHSM L=50-100 MHz M=100-500 MHz
* BLUE CELL™ mixers protected by U.S. Patents 5,534,830 5,640,132 5,640,134 5,640,699
** Protected under U.S. Patent 6133525
*** Prices for quantities 10-49
A. Environmental specifications and re-flow soldering information available in General Information Section.
B. Units are non-hermetic unless otherwise noted. For details on case dimensions & finishes see "Case Styles & Outline Drawings".
C. Prices and Specifications subject to change without notice.
1. Absolute maximum power, voltage and current ratings:
1a. RF power 200mW; 1b. Peak IF current, 40mA

NSN GUIDE

MCL NO.	NSN
ROK-186MH	5895-01-392-2276
SRA-1MH	5895-01-391-0113
TFM-3MH	5895-01-302-7047
TFM-42MH	5895-01-408-6093

020729


† RMS


SKY


SYM


TUF-SM

+13 dBm LO, up to +9 dBm RF

◆ MODEL NO.	FREQUENCY MHz LO/RF f_L-f_U	IF	CONVERSION LOSS dB Mid-Band m $\bar{x}$	σ	Max.	Total Range Max.	LO-RF ISOLATION dB L Typ.	L Min.	M Typ.	M Min.	U Typ.	U Min.	LO-IF ISOLATION dB L Typ.	L Min.	M Typ.	M Min.	U Typ.	U Min.	IP3@ center band Typ. (dBm)	E factor	CASE STYLE	CONNECTION	PCB Lay-out PL-	PRICE $ Qty. (10-49)
RMS-1MH	2-500	DC-500	5.65	.08	7.0	8.0	58	45	44	25	30	20	55	40	36	25	28	17	26	1.3	TT240	w	052	8.95
RMS-2MH	5-1000	DC-1000	6.72	.08	8.5	9.5	55	40	39	20	22	16	52	35	30	17	18	12	—		TT100	w	052	9.95
RMS-5MH	10-1500	DC-900	5.67	.09	9.0	9.5	58	40	40	20	26	18	50	30	38	18	17	8	—		TT240	w	052	15.95
RMS-25MH	5-2500	5-1500	7.0	.20	8.5	9.8	54	28	32	23	32	20	34	23	32	25	28	17	17	0.4	TT240	w	052	9.95
NEW RMS-25MHW	5-2500	5-2200	7.0	0.1	8.5	9.8	54	28	32	23	32	20	34	23	32	25	28	17	17	0.4	TT240	w	052	7.95
JRMS-42MH	800-4200	DC-800	5.3	.20	9.0	10.8	35	25	—	—	28	17	18	10	—	—	15	7	—		TT240	w	052	24.95
SKY-53MHR	2800-5300	DC-500	5.7	.20	—	9.5	28 (Typ.)	15 (Min.)					12 (Typ.)	8 (Min.)					19	0.6	BJ398	hp		17.95
SKY-60MH	2500-6000	DC-1500	6.2	.20	—	9.5	28 (Typ.)	17 (Min.)					14 (Typ.)	8 (Min.)					19	0.6	BJ398	je		17.95
SYM-11MH	50-2000	50-1000	6.6	.10	8.0	9.9	55	35	44	25	30	20	40	25	36	20	29	20	—		TTT167	x		15.95
SYM-25DMHW	40-2500	DC-1000‡	6.6	.10	8.0	9.0	47	32	37	27	35	22	38	28	35	25	38	20	26	1.3	TTT167	x		8.95***
SYM-1020MH	1000-2000	DC-800	6.5	.55	—	9.8	32 (Typ.)	20 (Min.)					20 (Typ.)	10 (Min.)					18	0.5	TTT167	lq		9.95
SYM-8022MH	800-2200	DC-800	7.6	0.3	—	9.8	26 (Typ.)	18 (Min.)					20 (Typ.)	9 (Min.)					18	0.5	TTT167	lp		11.95
TUF-1MHSM	2-600	DC-600	6.3	.12	7.0	8.0	68	50	50	30	43	25	65	45	48	30	37	22	15	0.2	NNN150	z		8.25
✪ TUF-2MHSM	50-1000	DC-1000	6.0	.25	7.5	9.0	58	40	47	30	37	25	55	35	47	20	32	18	—		NNN150	z		9.20
TUF-3MHSM	0.15-400	DC-400	5.0	.33	7.0	8.0	60	50	46	30	35	25	60	40	42	25	35	20	—		NNN150	z		10.20
TUF-5MHSM	20-1500	DC-1000	7.0	.25	8.5	9.0	50	40	41	30	35	25	38	25	28	18	20	8	—		NNN150	z		13.45
TUF-11AMHSM	1400-1900	40-500	7.4	.20	8.6	8.6	33 (Typ.)	20 (Min.)					24 (Typ.)	15 (Min.)					—		NNN150	z		21.95
TUF-2500MHSM	400-2500	30-800	7.3	.15	8.5	10.0	32 (Typ.)	24 (Min.)					27 (Typ.)	17 (Min.)					—		NNN150	z		21.95

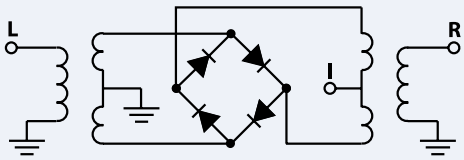
E= [IP3(dBm)-LO Power(dBm)]/10

L = low range [f_L to 10 f_L]

M = mid range [10 f_L to f_U/2]

m = mid band [2f_L to f_U/2]

U = upper range [f_U/2 to f_U]



pin and coaxial connections see case style outline drawings

PORT	w	x	z	hp	ht	je	jy	lc	ld	lp	lq
LO	1	2	4	5	6	1	1	10	10	3	3
RF	4	1	1	1	3	5	6	5	5	1	2
IF	5	3	2	7	2	7	10	3	3	2	1
GND EXT.	2,3,6	4,5,6	3	2,3,4,6,8	1,4,5	2,3,4,6,8	all others	1,4,7,8,9	1,2,4,6,7,8,9	4,5,6	4,5,6
ISOLATE	—	—	—	—	—	—	—	2,6	—	—	—
DEMO BOARD	TB-03	TB-12	—	TB-11	TB-03	TB-11	—	TB-117	TB-99 (MBA) TB-144 (MCA1)	—	—

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