DOCUMENTATION TECHNIQUE

Option B : électrotechnique

Contenu de la documentation technique :

- Circuit programmable CY7C374i
- Circuit PROM CY7C235A
- Convertisseur N/A AD7801
- Amplificateur opérationnel OP-470
- Circuits 'mélangeur'



UltraLogic[™] 128-Macrocell Flash CPLD

Features

- 128 macrocells in eight logic blocks
- 64 I/O pins
- 5 dedicated inputs including 4 clock pins
- In-System Reprogrammable™ (ISR™) Flash technology
 - JTAG interface
- · Bus Hold capabilities on all I/Os and dedicated inputs
- · No hidden delays
- High speed

 $-f_{MAX} = 125 \text{ MHz}$

— t_{PD} = 10 ns

—t_S = 5.5 ns

- —t_{CO} = 6.5 ns
- Fully PCI compliant
- 3.3V or 5.0V I/O operation
- Available in 84-pin PLCC, 84-pin CLCC, and 100-pin TQFP packages
- Pin compatible with the CY7C373i

Functional Description

The CY7C374i is an In-System Reprogrammable Complex Programmable Logic Device (CPLD) and is part of the FLASH370iTM family of high-density, high-speed CPLDs. Like all members of the FLASH370i family, the CY7C374i is designed to bring the ease of use as well as PCI Local Bus Specification support and high performance of the 22V10 to high-density CPLDs.

Like all of the UltraLogic[™] FLASH370i devices, the CY7C374i is electrically erasable and In-System Reprogrammable (ISR), which simplifies both design and manufacturing flows, thereby reducing costs. The Cypress ISR function is implemented through a JTAG serial interface. Data is shifted in and out through the SDI and SDO pin. The ISR interface is enabled using the programming voltage pin (ISR_{EN}). Additionally, because of the superior routability of the FLASH370i devices, ISR often allows users to change existing logic designs while simultaneously fixing pinout assignments.

The 128 macrocells in the CY7C374i are divided between eight logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.



Selection Guide

	7C374i-125	7C374i-100	7C374i-83	7C7374iL-83	7C374i-66	7C374iL-66
Maximum Propagation Delay ^[1] , t _{PD} (ns)	10	12	15	15	20	20
Minimum Set-Up, t _S (ns)	5.5	6	8	8	10	10
Maximum Clock to Output ^[1] , t _{CO} (ns)	6.5	7	8	8	10	10
Typical Supply Current, I _{CC} (mA)	125	125	125	75	125	75

Note:

1. The 3.3V I/O mode timing adder, $t_{3.3IO}$, must be added to this specification when V_{CCIO} = 3.3V.

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Pin Configurations





Pin Configurations (continued)





Functional Description (continued)

The logic blocks in the FLASH370i architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

Like all members of the FLASH370i family, the CY7C374i is rich in I/O resources. Every two macrocells in the device feature an associated I/O pin, resulting in 64 I/O pins on the CY7C374i. In addition, there is one dedicated input and four input/clock pins.

Finally, the CY7C374i features a very simple timing model. Unlike other high-density CPLD architectures, there are no hidden speed delays such as fanout effects, interconnect delays, or expander delays. Regardless of the number of resources used or the type of application, the timing parameters on the CY7C374i remain the same.

Logic Block

The number of logic blocks distinguishes the members of the FLASH370i family. The CY7C374i includes eight logic blocks. Each logic block is constructed of a product term array, a product term allocator, and 16 macrocells.

Product Term Array

The product term array in the FLASH370i logic block includes 36 inputs from the PIM and outputs 86 product terms to the product term allocator. The 36 inputs from the PIM are available in both positive and negative polarity, making the overall array size 72 x 86. This large array in each logic block allows for very complex functions to be implemented in single passes through the device.

Product Term Allocator

The product term allocator is a dynamic, configurable resource that shifts product terms to macrocells that require them. Any number of product terms between 0 and 16 inclusive can be assigned to any of the logic block macrocells (this is called product term steering). Furthermore, product terms can be shared among multiple macrocells. This means that product terms that are common to more than one output can be implemented in a single product term. Product term steering and product term sharing help to increase the effective density of the FLASH370i CPLDs. Note that product term allocation is handled by software and is invisible to the user.

I/O Macrocell

Half of the macrocells on the CY7C374i have I/O pins associated with them. The input to the macrocell is the sum of between 0 and 16 product terms from the product term allocator. The I/O macrocell includes a register that can be optionally bypassed, polarity control over the input sum-term, and two global clocks to trigger the register. The macrocell also features a separate feedback path to the PIM so that the register can be buried if the I/O pin is used as an input.

Buried Macrocell

The buried macrocell is very similar to the I/O macrocell. Again, it includes a register that can be configured as combinatorial, as a D flip-flop, a T flip-flop, or a latch. The clock for this register has the same options as described for the I/O macrocell. One difference on the buried macrocell is the addition of input register capability. The user can program the buried macrocell to act as an input register (D-type or latch)

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whose input comes from the I/O pin associated with the neighboring macrocell. The output of all buried macrocells is sent directly to the PIM regardless of its configuration.

Programmable Interconnect Matrix

The Programmable Interconnect Matrix (PIM) connects the eight logic blocks on the CY7C374i to the inputs and to each other. All inputs (including feedbacks) travel through the PIM. There is no speed penalty incurred by signals traversing the PIM.

Programming

For an overview of ISR programming, refer to the FLASH370i Family data sheet and for ISR cable and software specifications, refer to ISR data sheets. For a detailed description of ISR capabilities, refer to the Cypress application note, "An Introduction to In System Reprogramming with FLASH370i."

PCI Compliance

The FLASH370i family of CMOS CPLDs are fully compliant with the PCI Local Bus Specification published by the PCI Special Interest Group. The simple and predictable timing model of FLASH370i ensures compliance with the PCI AC specifications independent of the design. On the other hand, in CPLD and FPGA architectures without simple and predictable timing, PCI compliance is dependent upon routing and product term distribution.

3.3V or 5.0V I/O Operation

The FLASH370i family can be configured to operate in both 3.3V and 5.0V systems. All devices have two sets of V_{CC} pins: one set, V_{CCINT}, for internal operation and input buffers, and another set, V_{CCIO}, for I/O output drivers. V_{CCINT} pins must always be connected to a 5.0V power supply. However, the V_{CCIO} pins may be connected to either a 3.3V or 5.0V power supply, depending on the output requirements. When V_{CCIO} pins are connected to a 5.0V source, the I/O voltage levels are compatible with 5.0V systems. When V_{CCIO} pins are connected to a 3.3V source, the input voltage levels are compatible with 5.0V and 3.3V systems, while the output voltage levels are compatible with 3.3V systems. There will be an additional timing delay on all output buffers when operating in 3.3V I/O mode. The added flexibility of 3.3V I/O capability is available in commercial and industrial temperature ranges.

Bus Hold Capabilities on all I/Os and Dedicated Inputs

In addition to ISR capability, a new feature called bus-hold has been added to all FLASH370i I/Os and dedicated input pins. Bus-hold, which is an improved version of the popular internal pull-up resistor, is a weak latch connected to the pin that does not degrade the device's performance. As a latch, bus-hold recalls the last state of a pin when it is three-stated, thus reducing system noise in bus-interface applications. Bus-hold additionally allows unused device pins to remain unconnected on the board, which is particularly useful during prototyping as designers can route new signals to the device without cutting trace connections to V_{CC} or GND.

Design Tools

Development software for the CY7C371i is available from Cypress's *Warp*[™], *Warp* Professional[™], and *Warp* Enterprise[™] software packages. Please refer to the data sheets on these products for more details. Cypress also actively supports almost all third-party design tools. Please refer to third-party tool support for further information.



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage to Ground Potential	–0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Program Voltage	12.5V
Output Current into Outputs	16 mA

Static Discharge Voltage	.>2001V
(per MIL-STD-883, Method 3015)	

Latch-Up Current......>200 mA

Operating Range

Range	Ambient Temperature	V _{CC} V _{CCINT}	V _{CCIO}
Commercial	0°C to +70°C	5V ± 0.25V	$5V \pm 0.25V \\ OR \\ 3.3V \pm 0.3V$
Industrial	–40°C to +85°C	5V ± 0.5V	$5V \pm 0.5V \\ OR \\ 3.3V \pm 0.3V$
Military ^[2]	–55°C to +125°C	$5V\pm0.5V$	

Electrical Characteristics Over the Operating Range^[3, 4]

Parameter	Description		Test Conditions		Min.	Тур.	Max.	Unit
V _{OH}	Output HIGH Voltage	V_{CC} = Min.	I _{OH} = -3.2 mA (Com'l	/Ind) ^[5]	2.4			V
			$I_{OH} = -2.0 \text{ mA} (\text{Mil})$					V
V _{OHZ}	Output HIGH Voltage	$V_{CC} = Max.$	I _{OH} = 0 μA (Com'l/Ind) ^[5, 6]			4.0	V
	with Output Disabled ¹³		$I_{OH} = -50 \ \mu A \ (Com'I/I)$	nd) ^[5, 6]			3.6	V
V _{OL}	Output LOW Voltage	V_{CC} = Min.	I _{OL} = 16 mA (Com'l/In	ld) ^[5]			0.5	V
			I _{OL} = 12 mA (Mil)					V
V _{IH}	Input HIGH Voltage	Guaranteed I	nput Logical HIGH volta	age for all inputs ^[7]	2.0		7.0	V
V _{IL}	Input LOW Voltage	Guaranteed I	nput Logical LOW volta	ge for all inputs ^[7]	-0.5		0.8	V
I _{IX}	Input Load Current	V _I = Internal	GND, V _I = V _{CC}		-10		+10	μΑ
I _{OZ}	Output Leakage Current	V_{CC} = Max., V_{O} = GND or V_{O} = V_{CC} , Output Disabled			-50		+50	μA
		$V_{CC} = Max., V_{O} = 3.3V$, Output Disabled ^[6]				-70	-125	μA
I _{OS}	Output Short Circuit Current ^[8, 9]	V _{CC} = Max.,	V _{OUT} = 0.5V		-30		-160	mA
I _{CC}	Power Supply Current	$V_{CC} = Max.,$	I _{OUT} = 0 mA,	Com'l/Ind.		125	200	mA
		$f = 1 MHz, V_I$	_N = GND, V _{CC} ^[10]	Com'l "L" –66		75	125	mA
				Military		125	250	mA
I _{BHL}	Input Bus Hold LOW Sustaining Current	V _{CC} = Min., \	/ _{IL} = 0.8V		+75			μA
I _{BHH}	Input Bus Hold HIGH Sustaining Current	$V_{CC} = Min., V_{IH} = 2.0V$			-75			μA
I _{BHLO}	Input Bus Hold LOW Overdrive Current	V _{CC} = Max.					+500	μA
IBHHO	Input Bus Hold HIGH Overdrive Current	V _{CC} = Max.					-500	μA

Notes:

T_A is the "instant on" case temperature. 2.

5. 6.

See the last page of this specification for Group A subgroup testing information. If V_{CCIO} is not specified, the device can be operating in either 3.3V or 5V I/O mode; $V_{CC}=V_{CCINT}$. $I_{OH} = -2 \text{ mA}$, $I_{OL} = 2 \text{ mA}$ for SDO. When the I/O is three-stated, the bus-hold circuit can weakly pull the I/O to a maximum of 4.0V if no leakage current is allowed. This voltage is lowered significantly by a small leakage current. Note that all I/Os are three-stated during ISR programming. Refer to the application note "Understanding Bus Hold" for additional information. information.

These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
Not more than one output should be tested at a time. Duration of the short circuit should not exceed 1 second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
Tested initially and after any design or process changes that may affect these parameters.
Measured with 16-bit counter programmed into each logic block.

^{3.} 4.



Capacitance^[9]

Parameter	Description	Test Conditions	Min.	Max.	Unit
C _{I/O} ^[11, 12]	Input Capacitance	$V_{IN} = 5.0V$ at f = 1 MHz		8	pF
C _{CLK}	Clock Signal Capacitance	$V_{IN} = 5.0V$ at f = 1 MHz	5	12	pF

Inductance^[9]

Parameter	Description	Test Conditions	100-PinTQFP	84-Lead PLCC	84-Lead CLCC	Unit
L	Maximum Pin Inductance	$V_{IN} = 5.0V$ at f = 1 MHz	8	8	5	nH

Endurance Characteristics^[9]

Parameter	Description	Test Conditions	Max.	Unit
N	Maximum Reprogramming Cycles	Normal Programming Conditions	100	Cycles

AC Test Loads and Waveforms



Equivalent to:	THÉVENIN EQUIV	ALENT
	99Ω (COM'L)	
	136Ω (MIL)	2.08V (COM'L)
OUTPUT	00	2.13V (MIL)

Parameter ^[13]	V _X	Output Waveform Measurement Level
t _{ER(–)}	1.5V	
t _{ER(+)}	2.6V	V _{OH} V _X
t _{EA(+)}	1.5V	V _X V _{OH}
t _{EA(-)}	V _{thc}	V _X V _{OH}

Notes:

11. $C_{I\!/O}$ for the CLCC package are 12 pF Max

12. C_{I/O} for dedicated Inputs, and for I/O pins with JTAG functionality is 12 pF Max., and for ISR_{EN} is 15 pF Max.

13. t_{ER} measured with 5-pF AC Test Load and t_{EA} measured with 35-pF AC Test Load. Document #: 38-03031 Rev. **



Switching Characteristics Over the Operating Range^[14]

		7C374	li–125	7C37	4i–100	7C374i–83 7C374iL–83		7C374i–66 3 7C374iL–66		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Combinato	rial Mode Parameters									
t _{PD}	Input to Combinatorial Output ^[1]		10		12		15		20	ns
t _{PDL}	Input to Output Through Transparent Input or Output Latch ^[1]		13		15		18		22	ns
t _{PDLL}	Input to Output Through Transparent Input and Output Latches ^[1]		15		16		19		24	ns
t _{EA}	Input to Output Enable ^[1]		14		16		19		24	ns
t _{ER}	Input to Output Disable		14		16		19		24	ns
Input Regis	stered/Latched Mode Parameters									
t _{WL}	Clock or Latch Enable Input LOW Time ^[9]	3		3		4		5		ns
t _{WH}	Clock or Latch Enable Input HIGH Time ^[9]	3		3		4		5		ns
t _{IS}	Input Register or Latch Set-Up Time	2		2		3		4		ns
t _{IH}	Input Register or Latch Hold Time	2		2		3		4		ns
t _{ICO}	Input Register Clock or Latch Enable to Combinatorial Output ^[1]		14		16		19		24	ns
t _{ICOL}	Input Register Clock or Latch Enable to Output Through Transparent Output Latch ^[1]		16		18		21		26	ns
Output Reg	jistered/Latched Mode Parameters	1								
t _{CO}	Clock or Latch Enable to Output ^[1]		6.5		7		8		10	ns
t _S	Set-Up Time from Input to Clock or Latch Enable	5.5		6		8		10		ns
t _H	Register or Latch Data Hold Time	0		0		0		0		ns
t _{CO2}	Output Clock or Latch Enable to Output Delay (Through Memory Array) ^[1]		14		16		19		24	ns
t _{SCS}	Output Clock or Latch Enable to Output Clock or Latch Enable (Through Memory Array)	8		10		12		15		ns
t _{SL}	Set-Up Time from Input Through Transparent Latch to Output Register Clock or Latch En- able	10		12		15		20		ns
t _{HL}	Hold Time for Input Through Transparent Latch from Output Register Clock or Latch Enable	0		0		0		0		ns
f _{MAX1}	Maximum Frequency with Internal Feedback (Least of $1/t_{SCS}$, $1/(t_S + t_H)$, or $1/t_{CO}$) ^[9]	125		100		83		66		MHz
f _{MAX2}	Maximum Frequency Data Path in Output Registered/Latched Mode (Lesser of $1/(t_{WL} + t_{WH})$, $1/(t_{S} + t_{H})$, or $1/t_{CO}$)	158.3		143		125		100		MHz
f _{MAX3}	Maximum Frequency with External Feedback (Lesser of $1/(t_{CO} + t_S)$ and $1/(t_{WL} + t_{WH})$)	83.3		76.9		67.5		50		MHz
t _{OH} t _{IH} 37x	Output Data Stable from Output Clock Minus Input Register Hold Time for 7C37x ^[9, 15]	0		0		0		0		ns
Pipelined N	Iode Parameters									
t _{ICS}	Input Register Clock to Output Register Clock	8		10		12		15		ns
f _{MAX4}	Maximum Frequency in Pipelined Mode (Least of $1/(t_{CO} + t_{IS})$, $1/t_{ICS}$, $1/(t_{WL} + t_{WH})$, $1/(t_{IS} + t_{IH})$, or $1/t_{SCS}$)	125		100		83.3		66.6		MHz

Notes:

All AC parameters are measured with 16 outputs switching and 35-pF AC Test Load.
This specification is intended to guarantee interface compatibility of the other members of the CY7C370i family with the CY7C374i. This specification is met for the devices operating at the same ambient temperature and at the same power supply voltage.



Switching Characteristics Over the Operating Range^[14] (continued)

		7C374	li–125	7C374i–100		7C374i-83 7C374iL-83		7C374i-66 7C374iL-66		
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Reset/Pres	et Parameters									
t _{RW}	Asynchronous Reset Width ^[9]	10		12		15		20		ns
t _{RR}	Asynchronous Reset Recovery Time ^[9]	12		14		17		22		ns
t _{RO}	Asynchronous Reset to Output ^[1]		16		18		21		26	ns
t _{PW}	Asynchronous Preset Width ^[9]	10		12		15		20		ns
t _{PR}	Asynchronous Preset Recovery Time ^[9]	12		14		17		22		ns
t _{PO}	Asynchronous Preset to Output ^[1]		16		18		21		26	ns
Tap Contro	ller Parameter									
f _{TAP}	Tap Controller Frequency	500		500		500		500		kHz
3.3V I/O Mo	ode Parameters									
t _{3.3IO}	3.3V I/O mode timing adder		1		1		1		1	ns

Switching Waveforms





Switching Waveforms (continued)







Switching Waveforms (continued)

Asynchronous Reset





Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
125	CY7C374i-125AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C374i-125JC	J83	84-Lead Plastic Leaded Chip Carrier	
100	CY7C374i-100AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C374i-100JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C374i-100AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C374i-100JI	J83	84-Lead Plastic Leaded Chip Carrier	
83	CY7C374i–83AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C374i–83JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C374i–83AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C374i–83JI	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C374i-83GMB	G84	84-Pin Ceramic Pin Grid Array	Military
	CY7C374i-83YMB	Y84	84-Pin Ceramic Leaded Chip Carrier	
	CY7C374iL-83AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C374iL-83JC	J83	84-Lead Plastic Leaded Chip Carrier	
66	CY7C374i–66AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C374i–66JC	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C374i–66AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C374i–66JI	J83	84-Lead Plastic Leaded Chip Carrier	
	CY7C374i–66GMB	G84	84-Pin Ceramic Pin Grid Array	Military
	CY7C374i–66YMB	Y84	84-Pin Ceramic Leaded Chip Carrier	
	CY7C374iL-66AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C374iL-66JC	J83	84-Lead Plastic Leaded Chip Carrier	

MILITARY SPECIFICATIONS Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL}	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC1}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t _{PD}	9, 10, 11
t _{PDL}	9, 10, 11
t _{PDLL}	9, 10, 11
t _{CO}	9, 10, 11
t _{ICO}	9, 10, 11
t _{ICOL}	9, 10, 11
t _S	9, 10, 11
t _{SL}	9, 10, 11
t _H	9, 10, 11
t _{HL}	9, 10, 11
t _{IS}	9, 10, 11
t _{IH}	9, 10, 11
t _{ICS}	9, 10, 11
t _{EA}	9, 10, 11
t _{ER}	9, 10, 11



Package Diagrams







Package Diagrams (continued)









Package Diagrams (continued)



84-Pin Ceramic Leaded Chip Carrier Y84

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Document Title: cy7c374iUltraLogic™ 128-Macrocell Flash CPLD Document Number: 38-03031						
REV. ECN NO. Date Orig. of Change Description of Change						
**	106376	07/11/01	SZV	Change from Spec number: 38-00496 to 38-03031		



CY7C235A

Features

- CMOS for optimum speed/power
- High speed
 - —18 ns address set-up
- -12 ns clock to output
- Low power
 - -495 mW (commercial)
 - 660 mW (military)
- Synchronous and asynchronous output enables
- On-chip edge-triggered registers
- Programmable asynchronous registers (INIT)
- EPROM technology, 100% programmable
- Slim, 300-mil, 24-pin plastic or hermetic DIP or 28-pin LCC and PLCC
- + 5V $\pm 10\%$ V_CC, commercial and military
- TTL-compatible I/O
- Direct replacement for bipolar PROMs

1K x 8 Registered PROM

 Capable of withstanding greater than 2001V static discharge

Functional Description

The CY7C235A is a high-performance 1024 word by 8 bit electrically programmable read only memory packaged in a slim 300-mil plastic or hermetic DIP, 28-pin leadless chip carrier, or 28-pin plastic leaded chip carrier. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C235A replaces bipolar devices pin for pin and offers the advantages of lower power, superior performance, and high programming yield. The EPROM cell requires only 12.5V for the supervoltage, and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that the product will meet AC specification limits after customer programming.



Selection Guide

		7C235A-18	7C235A-25	7C235A-30	7C235A-40
Minimum Address Set-Up Time (ns)		18	25	30	40
Maximum Clock to Output (ns)		12	12	15	20
Maximum Operating	Commercial	90	90	90	90
Current (mA)	Military		120	120	120

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)



Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12 for DIP)	–0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	–0.5V to +7.0V
DC Input Voltage	3.0V to +7.0V
DC Program Voltage (Pins 7, 18, 20 for	DIP)13.0V

Static Discharge Voltage	.>2001V
(per MIL-STD-883, Method 3015)	

Latch-Up Current......>200 mA

Operating Range

Range	Ambient Range Temperature			
Commercial	0°C to +70°C	5V ±10%		
Industrial ^[1]	-40°C to +85°C	5V ±10%		
Military ^[2]	–55°C to +125°C	5V ±10%		

Electrical Characteristics Over Operating Range^[3]

Parameter	Description	Test Conditions		Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = -4.0 mA V_{IN} = V_{IH} or V_{IL}	2.4		V	
V _{OL}	Output LOW Voltage	$V_{CC} = Min., I_{OL} = 16 mA$ $V_{IN} = V_{IH} \text{ or } V_{IL}$		0.4	V	
V _{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Vo Inputs ^[4]	Itage for All	2.0		V
V _{IL}	Input LOW Level	Guaranteed Input Logical LOW Vo Inputs ^[4]		0.8	V	
I _{IX}	Input Leakage Current	$GND \leq V_{IN} \leq V_{CC}$	-10	+10	μA	
V _{CD}	Input Clamp Diode Voltage	Note 5				
I _{OZ}	Output Leakage Current	$GND \leq V_{OUT} \leq V_{CC}$ Output Disat	-10	+10	μA	
I _{OS}	Output Short Circuit Current	$V_{CC} = Max., V_{OUT} = 0.0V^{[6]}$		-20	-90	mA
I _{CC}	Power Supply Current	I _{OUT} = 0 mA, C	ommercial		90	mA
		V _{CC} = Max.	ilitary		120	
V _{PP}	Programming Supply Voltage			12	13	V
I _{PP}	Programming Supply Current				50	mA
V _{IHP}	Input HIGH Programming Voltage			3.0		V
V _{ILP}	Input LOW Programming Voltage				0.4	V

Capacitance^[5]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	$T_A = 25^{\circ}C, f = 1 \text{ MHz}, V_{CC} = 5.0 \text{ V}$	10	pF
C _{OUT}	Output Capacitance		10	pF

Notes:

1.

2.

3. 4. 5. 6.

Contact a Cypress representative for industrial temperature range specifications.
T_A is the "instant on" case temperature.
See the last page of this specification for Group A subgroup testing information.
For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
See Introduction to CMOS PROMs in this Data Book for general information on testing.
For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.



AC Test Loads and Waveforms^[5]





Operating Modes

The CY7C235A incorporates a D-type, master-slave register on chip, reducing the cost and size of pipelined microprogrammed systems and applications where accessed PROM data is stored temporarily in a register. Additional flexibility is provided with synchronous (\overline{E}_S) and asynchronous (\overline{E}) output enables and asynchronous initialization (\overline{INIT}).

Upon power-up, the synchronous enable ($\overline{E}S$) flip-flop will be in the set condition causing the outputs ($O_0 - O_7$) to be in the OFF or high-impedance state. Data is read by applying the memory location to the address input ($A_0 - A_9$) and a logic LOW to the enable (\overline{E}_S) input. The stored data is accessed and loaded into the master flip-flops of the data register during the address set-up time. At the next LOW-to-HIGH transition of the clock (CP), data is transferred to the slave flip-flops, which drive the output buffers, and the accessed data will appear at the outputs ($O_0 - O_7$), provided the asynchronous enable (\overline{E}) is also LOW.

The outputs may be disabled at any time by switching the asynchronous enable (\overline{E}) to a logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

Regardless of the condition of \overline{E} , the outputs will go to the OFF or high-impedance state upon the next positive clock edge after the synchronous enable (\overline{E}_S) input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will return the output to the active state if \overline{E} is LOW. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next LOW-to-HIGH transition of the clock. This unique feature allows the CY7C235A decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

System timing is simplified in that the on-chip edge-triggered register allows the PROM clock to be derived directly from the system clock without introducing race conditions. The on-chip register timing requirements are similar to those of discrete registers available in the market.

The CY7C235A has an asynchronous initialize input (INIT). The initialize function is useful during power-up and time-out sequences and can facilitate implementation of other sophisticated functions such as a built-in "jump start" address. When activated the initialize control input causes the contents of a user programmed 1025th 8-bit word to be loaded into the on-chip register. Each bit is programmable and the initialize function can be used to load any desired combination of 1s and 0s into the register. In the unprogrammed state, activating INIT will generate a register CLEAR (all outputs LOW). If all the bits of the initialize word are programmed, activating INIT performs a register PRESET (all outputs HIGH).

Applying a LOW to the $\overline{\text{INIT}}$ input causes an immediate load of the programmed initialize word into the master and slave flip-flops of the register, independent of all other inputs, including the clock (CP). The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable ($\overline{\text{E}}$) LOW.

When power is applied the (internal) synchronous enable flip-flop will be in a state such that the outputs will be in the high-impedance state. In order to enable the outputs, a clock must occur and the \overline{ES} input pin must be LOW at least a set-up time prior to the clock LOW-to-HIGH transition. The \overline{E} input may then be used to enable the outputs.

When the asynchronous initialize input, \overline{INIT} , is LOW, the data in the initialize byte will be asynchronously loaded into the output register. It will not, however, appear on the output pins until they are enabled, as described in the preceding paragraph.



		7C235A-18 7C235A-25 7C235		5A-30	7C23	5A-40				
Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t _{SA}	Address Set-Up to Clock HIGH	18		25		30		40		ns
t _{HA}	Address Hold from Clock HIGH	0		0		0		0		ns
t _{CO}	Clock HIGH to Valid Output		12		12		15		20	ns
t _{PWC}	Clock Pulse Width	12		12		15		20		ns
t _{SES}	E _S Set-Up to Clock HIGH	10		10		10		15		ns
t _{HES}	E _S Hold from Clock HIGH	5		5		5		5		ns
t _{DI}	Delay from INIT to Valid Output		20		25		25		35	ns
t _{RI}	INIT Recovery to Clock HIGH	15		20		20		20		ns
t _{PWI}	INIT Pulse Width	15		20		20		25		ns
t _{COS}	Inactive to Valid Output from Clock HIGH ^[7]		15		20		20		25	ns
t _{HZC}	Inactive Output from Clock HIGH ^[7]		15		20		20		25	ns
t _{DOE}	Valid Output from \overline{E} LOW		15		20		20		25	ns
t _{HZE}	Inactive Output from \overline{E} HIGH		15		20		20		25	ns

Switching Characteristics Over Operating Range^[3, 5]

Note:

7. Applies only when the synchronous (\overline{E}_S) function is used.

Switching Waveforms^[5]



Programming Information

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed

programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.



Table 1. Mode Selection

		Pin Function ^[8]							
	Read or Output Disable	$A_0, A_3 - A_9$	A ₁	A ₂	СР	Es	E	INIT	$O_7 - O_0$
Mode	Other	A_0,A_3-A_9	A ₁	A ₂	PGM	VFY	E	V _{PP}	$D_{7} - D_{0}$
Read		$A_0, A_3 - A_9$	A ₁	A ₂	Х	V _{IL}	V _{IL}	V _{IH}	$O_{7} - O_{0}$
Output Disab	ble	$A_0, A_3 - A_9$	A ₁	A ₂	Х	V _{IH}	Х	V _{IH}	High Z
Output Disab	ble	$A_0, A_3 - A_9$	A ₁	A ₂	Х	Х	V _{IH}	V _{IH}	High Z
Initialize		$A_0, A_3 - A_9$	A ₁	A ₂	Х	Х	V _{IL}	V _{IL}	Init Byte
Program		$A_0, A_3 - A_9$	A ₁	A ₂	V _{ILP}	V _{IHP}	V _{IHP}	V _{PP}	$D_{7} - D_{0}$
Program Ver	ify	$A_0, A_3 - A_9$	A ₁	A ₂	V _{IHP}	V _{ILP}	V _{IHP}	V _{PP}	$O_{7} - O_{0}$
Program Inhi	ibit	$A_0, A_3 - A_9$	A ₁	A ₂	V _{IHP}	V _{IHP}	V _{IHP}	V _{PP}	High Z
Intelligent Pre	ogram	$A_0, A_3 - A_9$	A ₁	A ₂	V _{ILP}	V _{IHP}	V _{IHP}	V _{PP}	$D_{7} - D_{0}$
Program Initi	alize Byte	$A_0, A_3 - A_9$	V _{PP}	V _{ILP}	V _{ILP}	V _{IHP}	V _{IHP}	V _{PP}	$D_{7} - D_{0}$
Blank Check		$A_0, A_3 - A_9$	A ₁	A ₂	V _{IHP}	V _{ILP}	V _{IHP}	V _{PP}	Zeros

Note:

8. X = "don't care" but not to exceed V_{CC} \pm 5%.







Typical DC and AC Characteristics



C235A-10



Ordering Information^[9]

Speed (ns)			Package		Operating
t _{SA}	t _{CO}	Ordering Code	Name	Package Type	Range
18	12	CY7C235A-18DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C235A-18JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C235A-18PC	P13	24-Lead (300-Mil) Molded DIP	
25	12	CY7C235A-25DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C235A-25JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C235A-25PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C235A-25DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C235A-25LMB	L64	28-Square Leadless Chip Carrier	
30	15	CY7C235A-30DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C235A-30JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C235A-30PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C235A-30DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C235A-30LMB	L64	28-Square Leadless Chip Carrier	
40	20	CY7C235A-40DC	D14	24-Lead (300-Mil) CerDIP	Commercial
		CY7C235A-40JC	J64	28-Lead Plastic Leaded Chip Carrier	
		CY7C235A-40PC	P13	24-Lead (300-Mil) Molded DIP	
		CY7C235A-40DMB	D14	24-Lead (300-Mil) CerDIP	Military
		CY7C235A-40LMB	L64	28-Square Leadless Chip Carrier	1

Note:

9. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

MILITARY SPECIFICATIONS Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL}	1, 2, 3
I _{IX}	1, 2, 3
l _{oz}	1, 2, 3
I _{CC}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
t _{SA}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{CO}	7, 8, 9, 10, 11



Package Diagrams



28-Lead Plastic Leaded Chip Carrier J64



51-85001-A



Package Diagrams (continued)



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